Compatibility Differences Between the UT80CXX196KD and UT80CRH196KDS

Table 1: Cross Reference of Applicable Products

Product Name:	SMD #:	Device Type:	Internal PIC Number:
UT80CRH196KD UT80C196KD	5962R98583 5962-98583	01 and 02	JD02A through JD02D
UT80CRH196KDS	5962*02523	01 and 02	KC01A through --

1.0 Overview

In September 2002, Aeroflex UTMC begins shipping a new version of the UT80CXX196KD (Aeroflex UTMC PIC# JD02*) under the new part number UT80CRH196KDS (PIC# KC01*). The UT80CRH196KDS supersedes the UT80CRH196KD. By correcting all known bugs in the UT80CXX196KD, increasing the radiation and single event performance and providing an advanced memory read/write signal, the UT80CRH196KDS is a supreme alternative to its older counterpart. The UT80CRH196KDS is built on a different gate array with new cell libraries than the UT80CXX196KD and has an alternate function to a pin with previously dedicated functionality. Therefore, the UT80CRH196KDS is not 100% compatible to the UT80CXX196KD in all applications. This application note serves to succinctly identify the primary differences between the two devices.

2.0 Comparison of the UT80CXX196KD and the UT80CRH196KDS

There are four key areas of difference between the UT80CXX196KD and the newer UT80CRH196KDS. These areas include:

1. Functional performance,
2. Functional pin compatibility,
3. DC electrical characteristics, and
4. Radiation performance.

By evaluating these differences, the design engineer should be able to determine if the UT80CRH196KDS is a suitable replacement for the UT80CXX196KD their application.

2.0.0 Functional Performance Differences

This section summarizes the functional deltas between the latest versions of the UT80CXX196KD and the UT80CRH196KDS. Simply put, this means that the UT80CRH196KDS corrects all known functional bugs in the UT80CXX196KD. The following is a table that summarizes the bugs that have been corrected in the UT80CRH196KDS. The table also provides a link to a related document for each bug. You can download these references to obtain detailed information regarding the associated bugs.

Table 2: Bug Fixes Going from UT80CXX996KD to UT80CRH196KDS

Bug Description:	Reference Document:
The UT80CXX196KD would fetch an instruction without asserting the INST pin following a bus hold cycle.	UT80196-KD-ERR-001 http://www.utmc.com/products/inst_pin_err.pdf
Indirect branch instructions corrupt the contents of the destination register.	UT80196-KD-ERR-002 http://www.utmc.com/products/indir_br_err.pdf
The BMOV instruction could only move a maximum of 2^{14} words.	UT80CXX196KD Datasheet Appendix A http://www.utmc.com/products/ut80196.pdf
The $\overline{\text{BREQ}}$ signal could assert one CLKOUT cycle before the $\overline{\text{HLDA}}$ assertion of the READY signal was high when the JD02D was prepared to release the bus.	UT80CXX196KD Datasheet Appendix A http://www.utmc.com/products/ut80196.pdf

2.0.1 Functional Pin Differences

The only functional pin difference between the UT80CXX196KD and the UT80CRH196KDS is an advanced read/write function that was added as an alternate function to EDAC check bit 5. The following table compares the two pin descriptions.

Table 3: Functional Pin Differences

Pin #	JD02D Definition			KC01A Definition		
	I/O Type	Function Name	Description	I/O Type	Function Name	Description
2	TB	ECB5	EDAC Check Bit 5. Asserting the $\overline{\text{EDACEN}}$ pin will cause the error detection and correction engine to pass the EDAC Check Bit 5 through pin 2 of the UT80CXX196KD	TO	ADV_RD_$\overline{\text{WR}}$	Advanced Read and $\overline{\text{Write}}$. This pin has multiplexed functionality coincident with the Address/Data bus multiplexing. When address information is output on the AD pins, ADV_RD_$\overline{\text{WR}}$ is output. When the data information is on the AD pins, ECB5 is an I/O. ADV_RD_$\overline{\text{WR}}$ is output high for an external memory read, and low for an external memory write cycle.
				TB	ECB5	EDAC Check Bit 5. Asserting the $\overline{\text{EDACEN}}$ pin will cause the error detection and correction engine to pass the EDAC Check Bit 5 through pin 2 of the UT80CRH196KDS during the data phase of an external memory cycle.

Because the advanced read and write signal on the UT80CRH196KDS shares the exact same timing as the multiplexed address and data bus, it is easy to interpret by your address decoder and is minimally invasive to the EDAC check bit memory bus. The only limitation presented by the advanced read and write signal for UT80CXX196KD sockets is that the EDAC check bit memory must not use “WRITE CONTROLLED” memory accesses. In a typical “WRITE CONTROLLED” memory access, the output enable on the memory is always active. As a result, unless the write signal is active, the data bus will not be tri-stated. This, in turn, causes bus contention with the advanced read and write signal on the UT80CRH196KDS.

2.0.2 DC Electrical Characteristic Differences

Because the UT80CRH196KDS is built using a different gate array with new cell libraries than the UT80CXX196KD, there are a number of DC electrical characteristic differences between the two versions. The following table summarizes these variations.

Table 4: DC Electrical Characteristics Comparison

SYMBOL	PARAMETER	JD02D			KC01			UNIT
		CONDITION	MIN.	MAX.	CONDITION	MIN.	MAX.	
V_H	Typical Range of Hysteresis RESET		0.9			0.6		V
V_{OL}	Low-level Output Voltage (CMOS load)	I_{OL} = 200µA		0.3	I_{OL} = 100µA		0.25	V
	(TTL load)	I_{OL} = 4.0mA		0.4	I_{OL} = 4.0mA		0.4	V
V_{OH}	High-level Output Voltage (CMOS load) (Standard outputs) (TTL load)	I_{OH} = -200µA	V_{DD}-.3		I_{OL} = -100µA	V_{DD}-.25		V
		I_{OH} = -4.0mA	3.8		I_{OL} = -4.0mA	2.4		V
I_{OH1}	High-level Output Current (Open drain outputs with pull-ups)	$V_{OH} = V_{DD}$ -.3	-20		$V_{OH} = V_{SS}$	-225	-20	µA
		$V_{OH} = V_{DD}$ -.9	-60					
I_{IH}	Logical 1 Input Current (Test mode entry avoidance)	Not Defined	Not Defined	Not Defined	$V_{IN} = V_{IH}$	-225	-20	µA
I_{LI}	I/O Leakage Current, standard inputs/outputs in Z state	$V_{IN} = V_{SS}$ or V_{DD}	-5	+5	$V_{IN} = V_{SS}$ or V_{DD}	-10	+10	µA
I_{LI1}	I/O Leakage Current, with pull-ups	$V_{IN} = V_{SS}$	-800	-150	$V_{IN} = V_{SS}$	-225	-20	µA
I_{LI2}	I/O Leakage Current, with pull-downs	$V_{IN} = V_{DD}$	200	1500	$V_{IN} = V_{DD}$	20	225	µA
I_{OS}	Short Circuit output current (except for pins listed in Note 5)	V_{DD} = 5.5V	-100	130	V_{DD} = 5.5V	-100	100	mA
I_{OS1}	Short Circuit output current on pins in Note 5	V_{DD} = 5.5V	-200	250	V_{DD} = 5.5V	-200	200	mA

2.0.3 Radiation Performance Differences

The final set of differences between the UT80CXX196KD and the UT80CRH196KDS lie in radiation performance characteristics that have been enhanced on the UT80CRH196KDS. The following tables summarizes the radiation characteristics of each device:

Table 5: Radiation Hardness Specifications

Parameter	UT80CXX196KD Value	UT80CRH196KDS Value	UNITS
Total Dose	1.0E5	3.0E5	rad(Si)
Onset LET Threshold	14.4	25	MeV-cm^2/mg
Neutron Fluence	1.0E14	1.0E14	n/cm^2
Saturated Cross-Section	3.66E-7	6.0E-7	cm^2/bit
Single Event Upset	4.9E-4	3.5048E-6	errors/device-day
Single Event Latchup	LET > 128	LET > 128	MeV-cm^2/mg

Table 6: Weibull and Device Parameters for Error-Rate Calculation

Weibull Parameters	UT80CXX196KD	UT80CRH196KDS	
	9674 Storage Elements	1482 Register Elements	8192 SRAM Storage Elements
Shape Parameter	1	1.3	4
Width Parameter	14	18.5	150
Structural Cross-Section	3.66E-7 cm^2/bit	1.5E-7 cm^2/bit	6.0E-7 cm^2/bit
Onset LET	14.4 MeV-cm^2/mg	48 MeV-cm^2/mg	25 MeV-cm^2/mg
Depletion Depth	0.8µm	0.8µm	0.5µm
Funnel Depth	1.45µm	1.45µm	0.5µm