

# UTMC Application Note

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## UT80CXX196KD MicroController (JD02\*) ALE Considerations

### Introduction:

The UT80CXX196KD microcontroller incorporates a multiplexed address and data bus. As a result, the microcontroller provides an Address Latch Enable (ALE) signal to clock an external address latch. The address latch is used to demultiplex the address information from the data bus during an external memory or I/O cycle. The UT80CXX196KD will automatically pulse the ALE signal (Low-High-Low) after it has placed valid, stable address information on the address/data bus.

### Potential ALE Anomaly:

The output drivers on the UT80CXX196KD have a higher current drive capability and faster slew rate than the Intel 80C196KD. The higher drive capability is a desirable trait for most circuit designs, however, it does have one drawback. When a large number of output signals simultaneously transition from high to low (i.e. AD[15:0] bus changing from FFFFh to 0000h), the large influx of current into the device is routed out of the device through only 4 ground pins. The impedance of these pins (although minimized by design) may allow a transitional rise in the ground plane potential of the device. This transitional glitch may cause an anomaly if it appears on device output signals such as ALE. Consequently, an ALE glitch could clock latches in the system forcing them to capture false information on the address/data bus.

### Anomaly Mitigating Design Considerations:

1. Keep the capacitance on the AD[15:0] bus as low as possible. The UT80CXX196KD specifies a maximum of 50pF per pin. Additional capacitance causes higher surge currents during the switching of the address/data bus. Furthermore, if the address/data bus is routed to an off-board connection, on-board buffering is suggested.
2. Ensure that the grounding pins are connected to the system ground plane with a very low impedance. PCB traces to vias should be as short and wide as possible. Placing the UT80CXX196KD into a socket adds impedance, and may allow a voltage difference between the device and the system ground plane.
3. Use decoupling capacitor pairs (0.01 $\mu$ F, 0.1 $\mu$ F) for each of the 4 ground pins on the UT80CXX196KD. Keep the capacitors as close as possible to the ground pins on the UT80CXX196KD. This will help support surge current capability at the ground pins, diminishing the voltage difference across the ground plane of the system. Additionally, it is recommended that you use a bulk capacitor (10 $\mu$ F-100 $\mu$ F) somewhere on the system board to reduce any droop in the +5V supply.
4. Ensure that the system ground plane is connected to any off-board systems with a very low impedance. If the system ground has a transient voltage rise with respect to an off-board system, any signals that are sensed off-board will appear to have a transient voltage rise as well.
5. Design the system printed circuit board with proper design techniques for critical signals. Give close attention to cross-coupling of the address/data bus onto critical signals such as the ALE. ALE should be isolated by providing ground traces adjacent to its PCB trace. Critical signals running parallel to the address/data bus should be avoided, or kept to a minimum parallel distance.
6. Design the system using series type termination on critical signals like ALE. By placing a matching impedance, for example a 68 $\Omega$  resistor, in series with the ALE signal, you will induce a small voltage drop across the resistor which causes the ALE signal to remain within the driven input's low input voltage spec. Furthermore, using the resistor in conjunction with the parasitic capacitance on the ALE signal will provide a filter mechanism for the high frequency voltage glitches on the signal line. Below are the simulation results of several termination techniques used on the ALE to minimize glitching.

UTMC ran HSPICE simulations with the 80CXX196KD buffer structure where the address/data bus and EDAC check bits simultaneously transition from 3FFFFFFh to 000000h (the worst case cause of ALE glitching). The ALE signal was modeled to include the package parasitics, a 98 $\Omega$  characteristic PCB trace of 4 inches (modeled

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with a 52nH inductance and 5.7pF capacitance), and a 50pF parasitic load capacitance. Additionally, the ALE driver has a source impedance of 30Ω typical that should be considered when selecting a termination resistor to match the characteristic line impedance. Note: The peak voltages seen in the simulation are based on a 1st order spice model and do not suggest a true magnitude of voltage glitches on ALE. There are numerous other factors that can affect the integrity of the ALE signal for any particular design, which are not included in this model. Instead, these results should be used to show the relationship of termination techniques to signal glitching.

**Table 1: ALE Termination Simulation Results**

Termination Characteristics	ALE Peak Voltage Seen at the Destination	Percent Improvement from Un-terminated Line
Un-terminated Line (Baseline)	1.1	N/A
Series 10Ω on ALE (40Ω effective termination)	0.949	14%
Series 68Ω on ALE (98Ω effective termination)	0.523	52%
98Ω + 100pF AC termination	0.842	23%
98Ω + 200pF AC termination	0.83	25%
98Ω + 500pF AC Termination	0.822	25%

From the above table of simulation results of various termination techniques on the ALE signal, you will notice that the best method is a total series termination resistance that is equal to the characteristic impedance of the PCB trace. Remember that the termination resistor plus the source on-resistance of the ALE driver (30Ω typical) should equal the characteristic PCB trace impedance.

7. Use a schmitt trigger buffer or inverter pair to filter the ALE signal provided by the UT80CXX196KD used for the Address/Data bus demultiplexing latch clock. The positive going threshold voltage on a schmitt triggered input is higher than a CMOS or TTL threshold. Therefore, a typical ALE glitch seen on the UT80CXX196KD output will be filtered before it reaches the clock input of the Address/Data bus demultiplexing latch. Figure 1 shows the standard ALE usage, and Figure 2 shows the schmitt trigger ALE filtering scheme for demultiplexing the Address/Data bus.

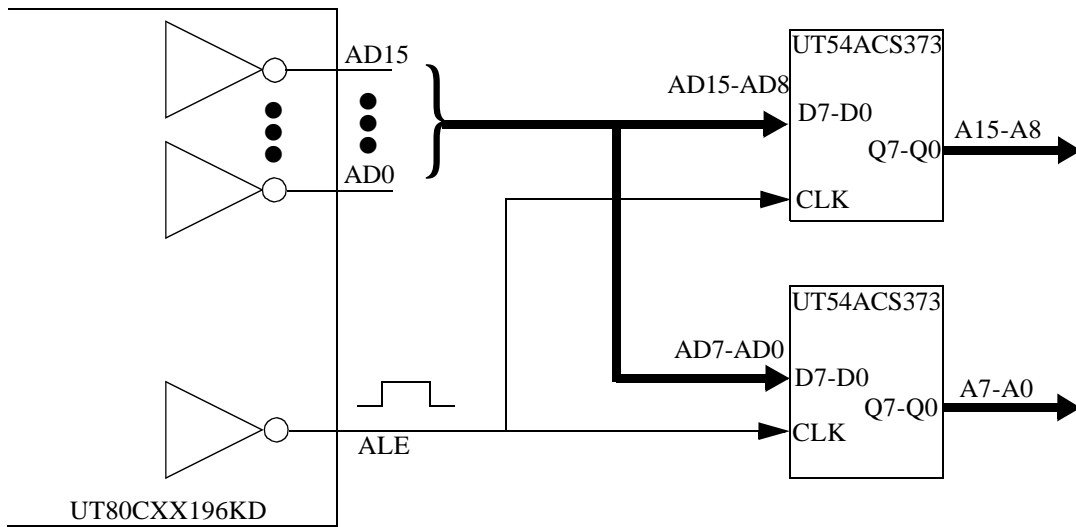


Figure 1. Typical Address/Data Bus Demultiplexing Scheme

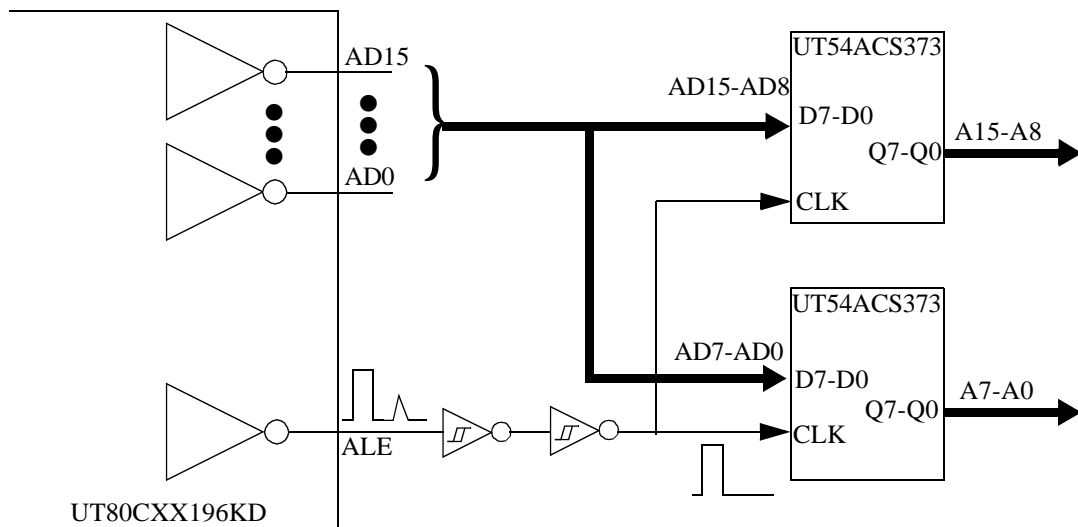


Figure 2. Address/Data Bus Demultiplexing Scheme with Schmitt Trigger ALE Filter