

EDA Design Tool Support



EDA Vendor	Software Package	Purpose
Synopsys	DesignCompiler PowerCompiler DFTCompiler TetraMax VHDLCompiler HDLCompiler PrimeTime VCS * VCS-MX * / Scirocco * Formality Astro Pro StarRC-XT	Logic Synthesis Power Synthesis / Analysis Test Circuitry Synthesis ATPG Read VHDL Designs Read Verilog Designs Sign-off Timing Analysis Verilog Simulation VHDL/Vital Simulation Formal Verification Place & Route Layout Extraction
Mentor Graphics	ModelSim * Leonardo Spectrum 3 QuickFault DesignArchitect FastScan **	VHDL & Verilog Simulation Logic Synthesis Fault grading Schematic entry ATPG
Cadence	Verilog-XL * Conformal / Verplex Encounter ** Dracula	Verilog Simulation Formal Verification Logic Synthesis Physical Verification

Notes:

In general, Aeroflex supports the most recent software versions but also maintains previous libraries.

* Aeroflex tested simulator. However models operate in any simulator that is OVI or VITAL compliant.

** Indirect support through conversion of Liberty formatted model files. Untested at Aeroflex.