Calculating Power Dissipation on LVDS Driver/Receiver Family

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC*
3.3-VOLT QUAD DRIVER	UT54LVDS031LV/E	5962-98651	02, 03, 04, 05	WD03, WD07, WD28, WD30
3.3-VOLT QUAD RECEIVER	UT54LVDS032LV/E	5962-98652	02, 03, 04, 05	WD04, WD08, WD29, WD31
3.3-VOLT QUAD RECEIVER with TERMINATION RESISTOR	UT54LVDS032LVT	5962-04201	01, 02	WD06, WD10
3.3V BUS QUAD DRIVER	UT54LVDM031LV	5962-06201	01	WD21
3.3V DUAL DRIVER and RECEIVER	UT54LVDM055LV	5962-06202	01	WD22
5.0V QUAD DRIVER	UT54LVDS031	5962-95833	02	JR05, JR08
5.0V QUAD RECEIVER	UT54LVDS032	5962-95834	02	JR06. JR09
5.0V QUAD DRIVER with COLD SPARE	UT54LVDSC031	5962-95833	03	JR10
5.0V QUAD RECEIVER with COLD SPARE	UT54LVDSC032	5962-95834	03	JR11

*PIC = Product Identification Code

1.0 Overview

Low Voltage Differential Signaling (LVDS) and bus Low Voltage Differential Signaling (LVDM) technologies are excellent solutions for moving large amounts of data quickly between system components. LVDS/LVDM systems run at high data rates, with low switching power, high noise immunity, and wide common mode range.

Accurate power calculations are necessary determine system power supply and thermal management requirements. The purpose of this application note is to review power consumption of Aeroflex Colorado Springs LVDS/LVDM driver and receiver families. To perform a thorough power analysis, it is necessary to investigate both static power consumption and “at frequency” or dynamic power consumption. Static power is the power dissipated under DC conditions when the part is powered, the drivers/receivers are enabled, but the device is not switching. Dynamic power consumption is due to the clocking and switching activity of the device.

This application note develops the components of LVDS/LVDM power consumption and example power dissipation calculations for typical LVDS/LVDM differential line drivers and receivers.

A standard point-to-point configuration is shown in Figure 1. This configuration is terminated by either a 100Ω or 35Ω resistor across the differential pair. Termination resistor selection is determined the differential signaling standard is used. LVDS requires a 100Ω resistor, while LVDM requires 35Ω. A constant current source feeds the differential outputs of the driver. The direction of current flow through the termination resistor (R_T) determines the logic state of the receiver output. In most cases (except when UT54LVDS032LVT is used) the termination is external to the receiver input terminals. Total power consumed by the standard point-to-point configuration is the device power minus the termination power. The LVDS output power consumption is a function of the output swing and the termination.

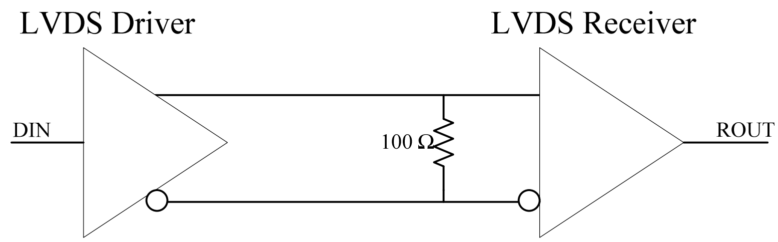

Figure 1. Standard point-to-point LVDS Driver Receiver Configuration

2.0 Technical Figures and Data

The following plots show active current, or *AIDD,* measurements versus frequency and are used as input current for calculating power dissipation and power dissipation capacitance(C_{PD}). The *AIDD* values are from maximum measurements taken during characterization of a single driver/receiver channel on each device configured under the following conditions.

Please note that the following data was obtained in a lab. The test setup does not match the test configurations shown for the AC and DC electrical characteristics described in the Aeroflex Datasheets and corresponding DSCC SMDs.

2.1 3.3V Device Data

Devices: UT54LVDS031LV/E, UT54LVDS032LV/E, UT54LVDS032LVT, UT54LVDM031LV, and UT54LVDM055LV

Temperature:	T_C = *25°C, +125°C, -55°C,*
Voltage:	V_{DD} =*3.3 V*
Frequency:	*f =1MHz, 50MHz, 100MHz, 150MHz, 200MHz*

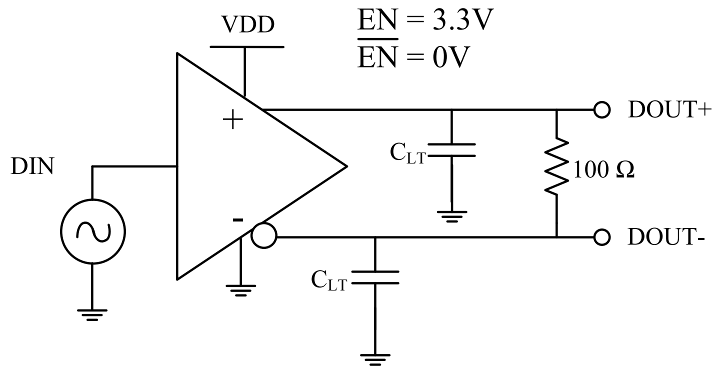

Figure 2A. LVDS Driver Test Configuration.
Unused drivers are driven low, meaning DIN = Vss

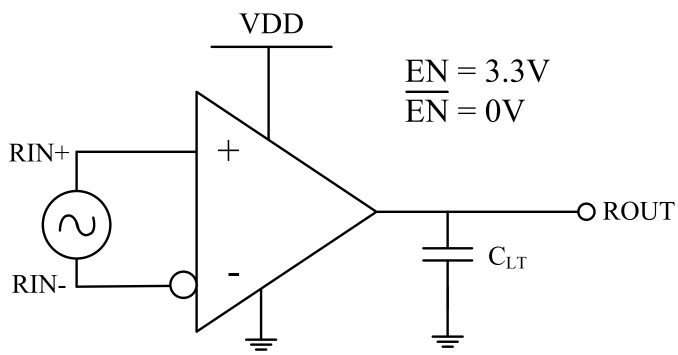

Figure 2B. LVDS Receiver Test Configuration.
Unused receivers have inputs floating, RIN+ = RIN- = FLOAT

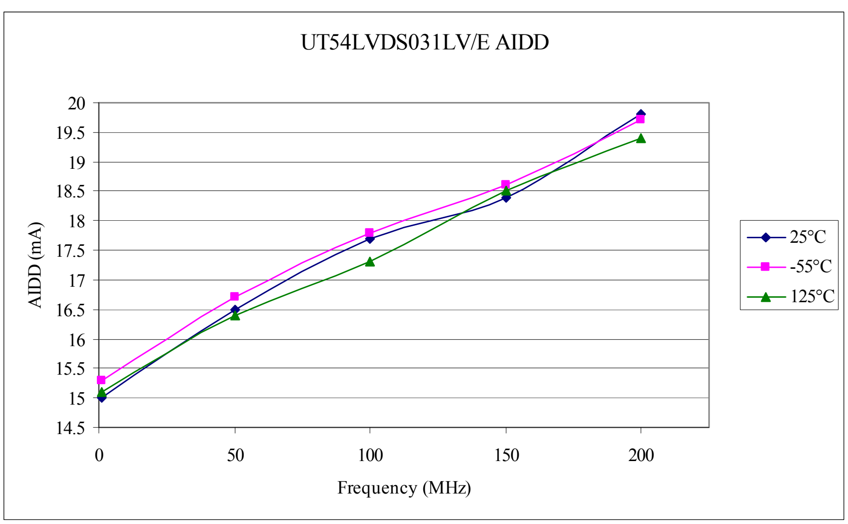

Figure 2. UT54LVDS031LV/E Active current vs. Frequency

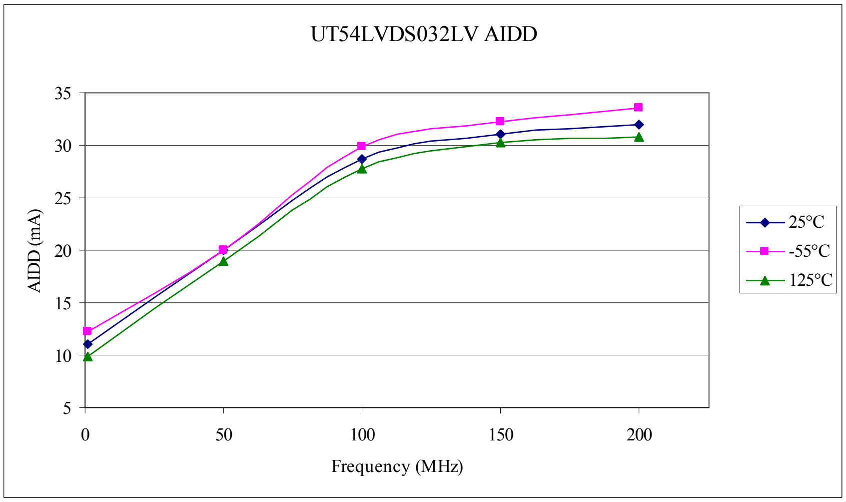

Figure 3. UT54LVDS032LV/E Active current vs. Frequency

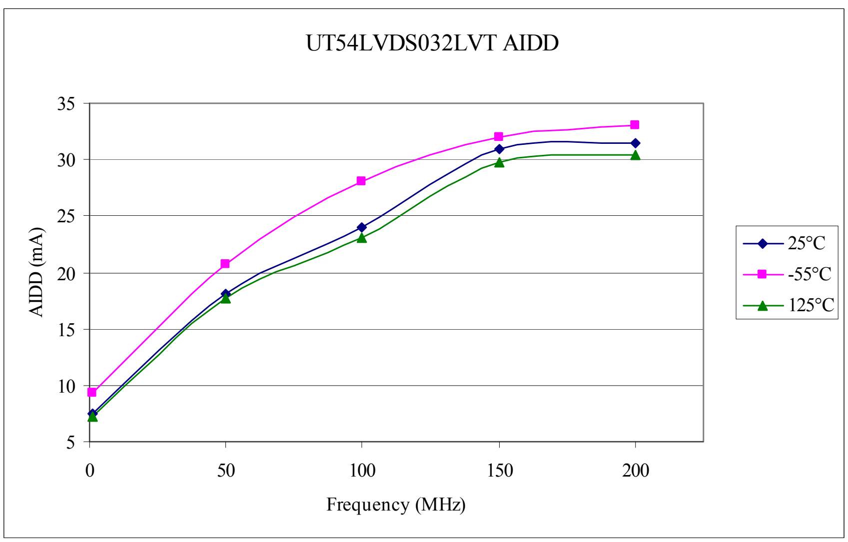

Figure 4. UT54LVDS032LVT Active current vs. Frequency

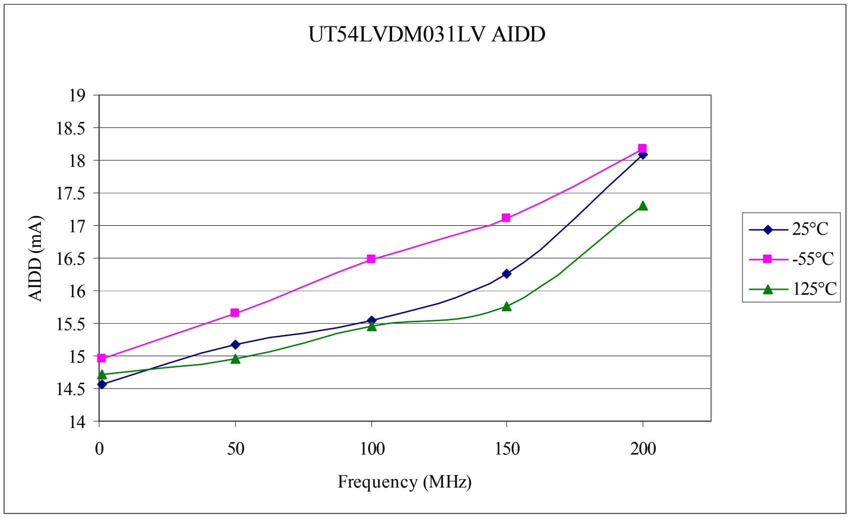

Figure 5. UT54LVDM031LV Active current vs. Frequency

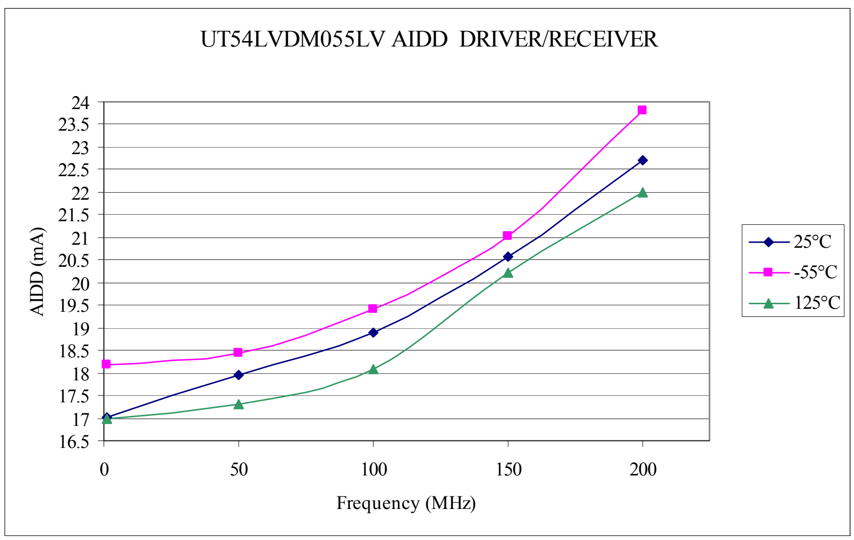

Figure 6. UT54LVDM055LV Active current vs. Frequency

Using the *AIDD* graphs provided above, or the data contained in tables 2 through 6 below, an estimate of the power supply current can be calculated by taking the slope of the line between two adjacent frequencies at a given temperature and multiplying by the user's desired frequency. The values in the "Slope (mA/MHz)" column are the values for the power supply input current that will be used in determining the power dissipation, power dissipation capacitance, and dynamic current consumption later in this application note.

Power dissipation capacitance or (C_{PD}) for the LVDS drivers was calculated using equation 1 as follows. It can be noted that the LVDS driver output switches only *340mV* which is approximately 10x less than $V_{DD} = 3.3V$ *or* $5.0V$, so C_{LT} can be neglected.

$$C_{PD} = \frac{Average(AIDD(slope))}{V_{DD}} \tag{1}$$

The C_{PD} value presented in Table 2 was calculated as follows in example 1.

2.1.1 Example 1

$$C_{PD} = \frac{Average(AIDD(slope))}{V_{DD}} = \frac{Average(0.0236, 0.221, 0.216)}{3.3V} = 6.81pF$$

C_{PD} for the LVDS receivers was calculated using equation 2 as follows. Since the LVDS receiver outputs switch rail to rail $V_{DD} = 3.3V$ *or* $5.0V$, C_{LT} must be accounted for.

$$C_{PD} = \frac{Average(AIDD(slope))}{V_{DD}} - C_{LT} \tag{2}$$

The C_{PD} value presented in Table 3 was calculated as follows in example 2.

2.1.2 Example 2

$$C_{PD} = \frac{Average(AIDD(slope))}{V_{DD}} - C_{LT} = \frac{Average(0.178, 0.178, 0.180)}{3.3} - 40pF = 14.37pF$$

Table 2.
UT54LVDS031LV/E Current vs. Frequency Data over Temperature with mA/MHz calculated

UT54LVDS031LV/E	Temperature (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD=3.3V	25	SIDD 0	15.0	
	25	1	15.1	
C_{LT}=20pF	25	50	16.5	0.028
	25	100	17.7	0.024
C_{PD}=6.81pF	25	150	18.4	0.014
	25	200	19.8	0.028
			Average Slope	= 0.0236
	-55	SIDD 0	15.2	
	-55	1	15.3	
	-55	50	16.7	0.028
	-55	100	17.8	0.022
	-55	150	18.6	0.016
	-55	200	19.7	0.022
			Average Slope	= 0.0221
	125	SIDD 0	15.0	
	125	1	15.1	
	125	50	16.4	0.026
	125	100	17.3	0.018
	125	150	18.5	0.024
	125	200	19.4	0.018
			Average Slope	= 0.0216

Table 3.
UT54LVDS032LV/E E Current vs. Frequency Data over Temperature with mA/MHz calculated

UT54LVDS032LV/E	Temperature (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD=3.3V	25	SIDD 0	10.9	
	25	1	11	
CLT=40pF	25	50	20	0.183
	25	100	28.7	0.174
CPD=14.37pF	25	150	31	0.046*
	25	200	32	0.02*
			Average Slope = 0.178	
	-55	SIDD 0	12.1	
	-55	1	12.2	
	-55	50	20	0.159
	-55	100	29.9	0.198
	-55	150	32.2	0.046*
	-55	200	33.5	0.026*
			Average Slope = 0.178	
	125	SIDD 0	9.8	
	125	1	9.9	
	125	50	18.9	0.183
	125	100	27.8	0.178
	125	150	30.3	0.05*
	125	200	30.8	0.01*
			Average Slope = 0.180	

* = These values were not included in the Average Slope calculation. These values were omitted because the output of the receiver was not swinging rail to rail.

Table 4.
UT54LVDS032LVT E Current vs. Frequency Data over Temperature with mA/MHz calculated

UT54LVDS032LVT	Temperature (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD=3.3V	25	SIDD 0	7.3	
	25	1	7.49	
C_{LT}=40pF	25	50	18.04	0.215
	25	100	24	0.119
C_{PD}=11.31pF	25	150	30.98	0.139
	25	200	31.43	0.009*
			Average Slope =0.158	
	-55	SIDD 0	9.1	
	-55	1	9.35	
	-55	50	20.77	0.233
	-55	100	28	0.144
	-55	150	32.01	0.080*
	-55	200	32.98	0.019*
			Average Slope =0.188	
	125	SIDD 0	7.08	
	125	1	7.2	
	125	50	17.67	0.213
	125	100	23.1	0.1086
	125	150	29.81	0.1342
	125	200	30.4	0.0118*
			Average Slope =0.161	

* = These values were not included in the Average Slope calculation. These values were omitted because the output of the receiver was not swinging rail to rail.

Table 5.
UT54LVDM031LV Current vs. Frequency Data over Temperature with mA/MHz calculated

UT54LVDM031LV	Temperature (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD=3.3V	25	SIDD 0	14.53	
	25	1	14.56	
CLT=20pF	25	50	15.17	0.0124
	25	100	15.54	0.0074
CPD=4.72pF	25	150	16.27	0.0146
	25	200	18.09	0.0364
			Average Slope = 0.017	
	-55	SIDD 0	14.9	
	-55	1	14.96	
	-55	50	15.65	0.0140
	-55	100	16.48	0.0166
	-55	150	17.1	0.0124
	-55	200	18.17	0.0214
			Average Slope = 0.016	
	125	SIDD 0	14.7	
	125	1	14.72	
	125	50	14.96	0.0048
	125	100	15.45	0.0098
	125	150	15.76	0.0062
	125	200	17.3	0.0308
			Average Slope = 0.013	

Table 6.
UT54LVDM055LV Current vs. Frequency Data over Temperature with mA/MHz calculated

UT54LVDM055LV	Temperature (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD=3.3V	25	SIDD 0	17	
	25	1	17.03	
	25	50	17.97	0.0191837
	25	100	18.9	0.0186
C_{LT}=20pF (DRIVER)	25	150	20.56	0.0332
C_{LT}=40pF (RECEIVER)	25	200	22.7	0.0428
			Average Slope =0.0284	
C_{PD}=8.25pF				
	-55	SIDD 0	17.23	
	-55	1	18.17	
	-55	50	18.44	0.0055102
	-55	100	19.4	0.0192
	-55	150	21.01	0.0322
	-55	200	23.81	0.056
			Average Slope =0.0282	
	125	SIDD 0	16.9	
	125	1	17	
	125	50	17.32	0.0065306
	125	100	18.1	0.0156
	125	150	20.21	0.0422
	125	200	22	0.0358
			Average Slope =0.025	

2.2 5.0V Device Data

Devices: UT54LVDS031, UT54LVDS032, UT54LVDSC031, and UT54LVDSC032

Temperature: $T_C = 25°C, +125°C, -55°C$
Voltage: $V_{DD} = 5.0\ V$
Frequency: f =1MHz, 25MHz, 50MHz, 75MHz, 100MHz

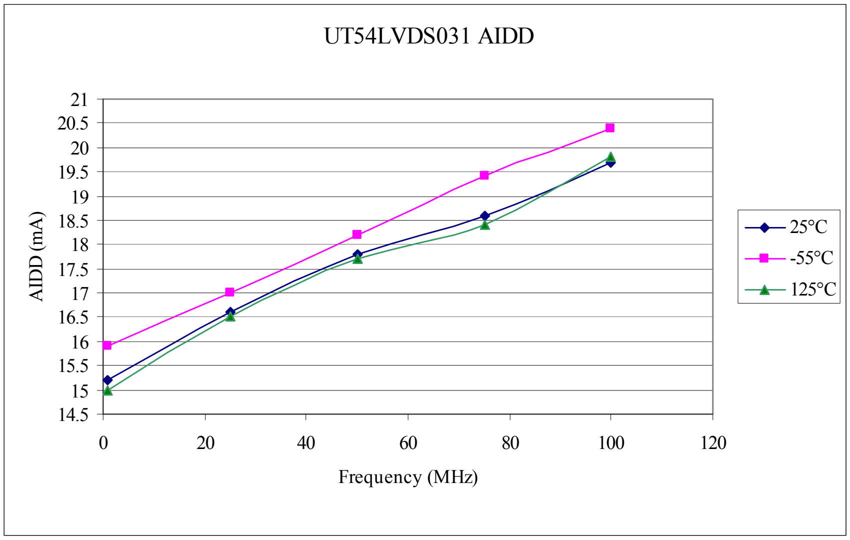

Figure 7. UT54LVDS031 Active current vs. Frequency

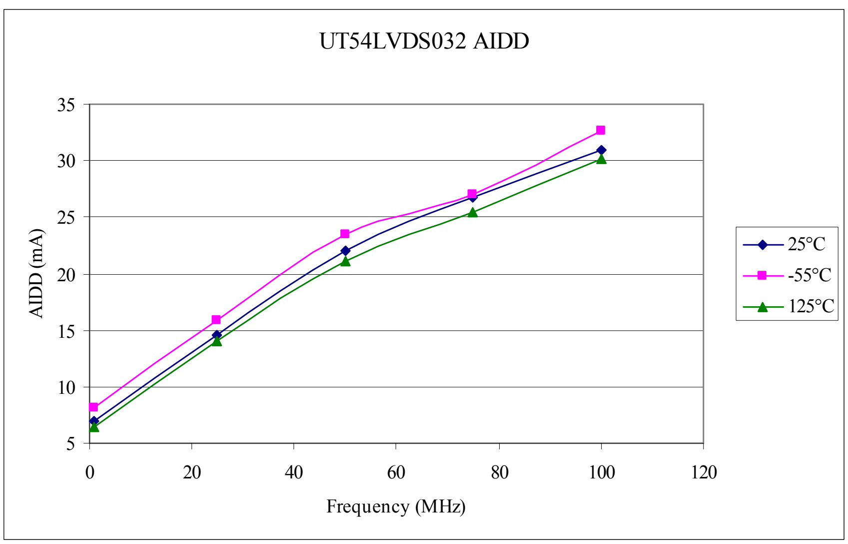

Figure 8. UT54LVDS032 Active current vs. Frequency

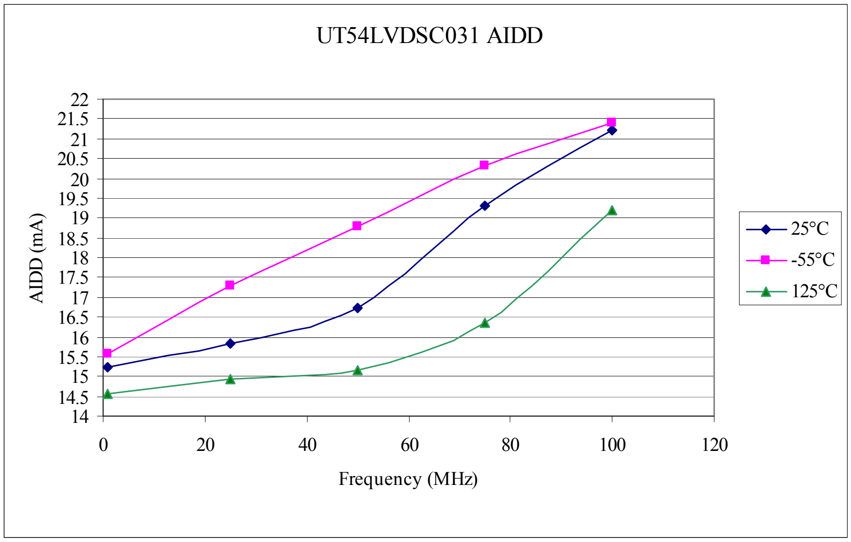

Figure 9. UT54LVDSC031 Active current vs. Frequency

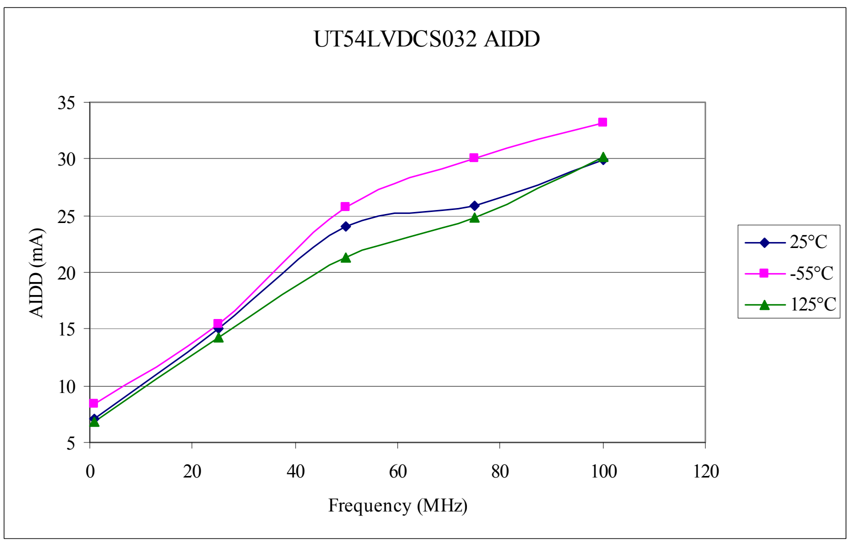

Figure 10. UT54LVDSC032 Active current vs. Frequency

Again, the device characterization data used to generate Figures 7 to 10 follows in Tables 7 through 10. Using the *AIDD* graphs provided above, or the data contained below, an estimate of the power supply current can be calculated by taking the slope of the lines at various frequencies.

Table 7.
UT54LVDS031 Current vs. Frequency Data over Temperature with mA/MHz calculated

UT54LVDS031	Temperature (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD=5.0V	25	SIDD 0	15.1	
	25	1	15.2	
C_{LT}=20pF	25	25	16.6	0.0583
	25	50	17.8	0.048
C_{PD}=9.31pF	25	75	18.6	0.032
	25	100	19.7	0.044
			Average Slope =0.046	
	-55	SIDD 0	15.8	
	-55	1	15.9	
	-55	25	17	0.0458
	-55	50	18.2	0.048
	-55	75	19.4	0.048
	-55	100	20.4	0.04
			Average Slope =0.045	
	125	SIDD 0	14.9	
	125	1	15.0	
	125	25	16.5	0.0625
	125	50	17.7	0.048
	125	75	18.4	0.028
	125	100	19.8	0.056
			Average Slope =0.048	

Table 8.
UT54LVDS032 Current vs. Frequency Data over Temperature with mA/MHz calculated

UT54LVDS032	Temperature (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD=5.0V	25	SIDD 0	6.8	
	25	1	7	
C_{LT}=40pF	25	25	14.5	0.3125
	25	50	22	0.3
C_{PD}=21.12pF	25	75	26.7	0.188*
	25	100	31	0.172*
			Average Slope =0.306	
	-55	SIDD 0	8	
	-55	1	8.2	
	-55	25	15.9	0.32083333
	-55	50	23.5	0.304
	-55	75	27	0.14*
	-55	100	32.7	0.228*
			Average Slope =0.312	
	125	SIDD 0	6.3	
	125	1	6.5	
	125	25	14	0.3125
	125	50	21.1	0.284
	125	75	25.4	0.172*
	125	100	30.2	0.192*
			Average Slope =0.298	

* = These values were not included in the Average Slope calculation. These values were omitted because the output of the receiver was not swinging rail to rail.

Table 9.
UT54LVDSC031 Current vs. Frequency Data over Temperature with mA/MHz calculated

UT54LVDSC031	Temperature (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD=5.0V	25	SIDD 0	15.16	
	25	1	15.23	
CLT=20pF	25	25	15.83	0.025
	25	50	16.72	0.0356
CPD=10.2pF	25	75	19.3	0.1032
	25	100	21.2	0.076
			Average Slope =0.0599	
	-55	SIDD 0	15.5	
	-55	1	15.56	
	-55	25	17.3	0.0725
	-55	50	18.78	0.0592
	-55	75	20.3	0.0608
	-55	100	21.4	0.044
			Average Slope =0.0591	
	125	SIDD 0	14.4	
	125	1	14.57	
	125	25	14.95	0.0158333
	125	50	15.16	0.0084
	125	75	16.35	0.0476
	125	100	19.18	0.1132
			Average Slope =0.046	

Table 10.
UT54LVDSC032 Current vs. Frequency Data over Temperature with mA/MHz calculated

UT54LVDS032	Temperature (°C)	Frequency (MHz)	AIDD (mA)	Slope (mA/MHz)
VDD=5.0V	25	SIDD 0	6.8	
	25	1	7.09	
CLT=40pF	25	25	15.04	0.3312
	25	50	24.03	0.3596
CPD=26.43pF	25	75	25.9	0.0748*
	25	100	29.87	0.1588*
			Average Slope =0.345	
	-55	SIDD 0	8.1	
	-55	1	8.34	
	-55	25	15.4	0.294
	-55	50	25.76	0.4144
	-55	75	30	0.1696*
	-55	100	33.21	0.1284*
			Average Slope =0.354	
	125	SIDD 0	6.53	
	125	1	6.77	
	125	25	14.2	0.3095
	125	50	21.3	0.284
	125	75	24.8	0.14*
	125	100	30.11	0.2124*
			Average Slope =0.296	

* = These values were not included in the Average Slope calculation. These values were omitted because the output of the receiver was not swinging rail to rail.

3.0 Calculating of Power with Variable Load Capacitance

The following equations and examples are provided as a guide for estimating static power dissipation, dynamic power dissipation, and power dissipation capacitance using various capacitive loads.

Definition of Terms:

V_{DD}	Supply Voltage (V)
V_{OD}	Differential Output Voltage, ±0.340V for Drivers/Receivers (V)
V_{OL}	Low-level output voltage (V)
$V_{OL}(actual)$	Load Dependant Low-level output voltage (V)
V_{OH}	High-level output voltage (V)
$V_{OH}(actual)$	Load Dependant High-level output voltage (V)
AIDD	Active Current (mA)
AIDD(slope)	Slope of AIDD (mA/MHz)
AIDD(frequency)	Active current at given frequency (mA)
SIDD	Standby Current Device Enabled f=0MHz (mA)
I_{OL}	Low level output current (mA)
I_{OH}	High level output current (mA)
I_{OD}	LVDS Driver Output Current (mA)
P_{DCL}	Percent Duty Cycle Driving Logic Low (%)
P_{DCH}	Percent Duty Cycle Driving Logic High (%)
N_{SWDP}	Number of switching differential pairs
N_O	Number of switching CMOS outputs
C_{PD}	Power Dissipation Capacitance (F)
C_L	Load Capacitance (F)
C_{LT}	Capacitive per switching output Tester Load (F)
f	Frequency (Hz)
P_{RLOAD}	Resistive Load Output Power (W)
P_{STD}	Static DC Power Dissipation for Driver (W)
P_{STR}	Static DC Power Dissipation for Receiver (W)
P_{DYND}	Dynamic Power Dissipation for Driver (W)
P_{DYNR}	Dynamic Power Dissipation for Receiver (W)
P_{TOTALD}	Total Driver Power Dissipation (W)
P_{TOTALR}	Total Receiver Power Dissipation (W)

Driver Static Power is the power the device consumes when enabled and V_{DD} is within the recommended operating conditions. Dynamic power is the power required to switch "N" number of LVDS/LVDM differential output pairs or single ended digital output loads. The total driver power is the static power plus the dynamic power plus the internal switching power at a given toggle frequency.

LVDS Driver Power Calculations:

Static Device Power (P_{STD}):

$$P_{STD} = SIDD * V_{DD} \quad (3)$$

Dynamic Power per Switching Driver (P_{DYND}):

$$P_{DYND} = \left(\left(C_{PD}\left(V_{DD}{}^{2} * f\right)\right) + \left(C_{L}\left(V_{DD} * V_{OD}\right) * f\right)\right) \quad (4)$$

Total Driver Power (P_{TOTALD}):

$$P_{TOTALD} = \left(P_{STD} + \left(N_{SWDP} * P_{DYND}\right)\right) = \left(SIDD * V_{DD}\right) + \left(N_{SWDP}\left[\left(C_{PD}\left(V_{DD}{}^{2} * f\right)\right) + \left(C_{L}\left(V_{DD} * V_{OD}\right) * f\right)\right]\right) \quad (5)$$

LVDS Receiver Power Calculations:

Static Device Power (P_{STR}):

$$P_{STR} = SIDD * V_{DD} \quad (6)$$

Resistive Output Load Power (P_{LOAD}):

$$P_{RLOAD} = \left[\left(P_{DCL} * V_{OL} * I_{OL}\right) + \left(P_{DCH} * \left(V_{DD} - V_{OH}\right) * \left|I_{OH}\right|\right)\right] \quad (7)$$

Dynamic Power per Switching Receiver (P_{DYNR}):

$$P_{DYNR} = \left(C_{PD}\left(V_{DD}{}^{2} * f\right)\right) + \left(C_{L}\left(V_{OH}(actual) - V_{OL}(actual)\right)^{2} * f\right) \quad (8)$$

Total Receiver Power (P_{TOTALR}):

$$P_{TOTALR} = P_{STR} + \left(N_{O}\left(P_{DYNR} + P_{RLOAD}\right)\right) \quad (9)$$

Table 11. LVDS Driver/Receiver DC Electrical Parameters [1,2]

LVDS Part ID	C_{LT}	I_{OD}	f (max)	V_{OL}[4]	V_{OH}[4]	I_{OH}[4]	I_{OL}[4]
UT54LVDS031	20pF	3.5mA	77.7MHz	0.90V	1.60V	--	--
UT54LVDS032	40pF	--	77.7MHz	0.3V	4.0V	-0.4mA	2.0mA
UT54LVDSC031	20pF	3.5mA	77.7MHz	0.90V	1.60V	--	--
UT54LVDSC032	40pF	--	77.7MHz	0.3V	4.0V	-0.4mA	2.0mA
UT54LVDS031LV/E	20pF	3.5mA	200MHz	0.925V	1.650V	--	--
UT54LVDS032LV/E	40pF	--	200MHz	0.25V	2.7V	-0.4mA	2.0mA
UT54LVDS032LVT	40pF	3.5mA	200MHz	0.25V	2.7V	--	--
UT54LVDM031LV	20pF	10mA	200MHz	0.855V	1.750V	--	--
UT54LVDM055LV[3]	20pF 40pF	10mA --	200MHz 200MHz	0.855V 0.25V	1.750V 2.7V	-- -0.4mA	-- 2.0mA

Notes:
1. All values are typical unless otherwise noted.
2. The top line contains specifications for the Driver, the bottom line for the Receiver.
3. Values are per the datasheet DC electrical characteristics.

4.0 Example Calculations

The following sections walk the designer through two example calculations using the data and equations presented in sections 2.0 and 3.0 above.

4.1 Example 3

The UT54LVDS031LV analysis assumes utilization of 2 driver channels switching at *170MHz* with *50pF* capacitive loads at 25°C.

UT54LVDS031LV Driver Power

$$V_{DD} = 3.3V$$
$$N_{SWDP} = 2$$
$$C_L = 50\,pF$$
$$AIDD(slope) = 0.028\text{mA/MHz}$$
$$\text{SIDD} = 15.0\text{mA (Table 2)}$$

$$V_{OD} = 0.340V$$
$$I_{OD} = .0035A$$
$$f = 170MHz$$
$$C_{PD} = 6.81pF \quad (Table\,2)$$

Static Device Power *(P_{STD})*:
Using equation (3):

$$P_{STD} = SIDD * V_{DD} = 15.0mA * 3.3V = 49.5\,mW$$

Dynamic Power per Active Driver *(P_{DYND})*:

$$P_{DYND} = \left(\left(C_{PD}\left(V_{DD}{}^{2} * f\right)\right) + \left(C_{L}\left(V_{DD} * V_{OD}\right) * f\right)\right) =$$
$$\left(\left(6.81pF\left(3.3V^{2} * 170MHz\right)\right) + \left(50pF\left(3.3V * 0.340V\right) * 170MHz\right)\right) =$$
$$12.61mW + 9.53mW = 22.14mW$$

Total Device Power Dissipation (P_{TOTALD}):

2 switching differential outputs:

$$P_{TOTALD} = P_{STD} + \left(N_{SWDP}\left(P_{DYND}\right)\right) = 49.56mW + \left(2\left(22.14mW\right)\right) = 93.78mW$$

Quickly comparing the measured data from table 2 using Joule's Law ($P{=}I*V$):

$$I = \left(AIDD(slope) * f * N_{SWDP}\right) + SIDD = \left(0.028mA / MHz * 170MHz * 2\right) + 15.0mA = 24.52mA$$

2 switching differential outputs:

$$P = I * V = 24.52mA * 3.3V = 80.92mW$$

If example 4 were recalculated using a C_L of *20pF*, a result of 82.34mW is obtained. Therefore, the C_{PD} form of the power calculation is within 2% of the Joule's Law form.

4.1 Example 4

The UT54LVDS032 analysis assumes utilization of all 4 receivers switching at *40MHz* (50/50 duty cycle), with a *20pF* capacitive load, and a *2.35kΩ* pull up on the CMOS output, at -55°C. A pull up resistor is present on the CMOS output of the receiver to pull up the output of the receiver if the enable signals disable and Z state the outputs (EN = L and /EN = H). In practice the bias resistor will be defined by the system designer.

$V_{DD} = 5.0V$

$C_L = 20pF$

$C_{PD} = 21.12pF\ (Table\ 8)$

$\mathrm{N_O} = 4$

$P_{DCL} = 0.5 \qquad P_{DCH} = 0.5$

$f = 40MHz$

$V_{OH}(actual) = 5.0V$

$V_{OL}(actual) = V_{DD} - (2.35k\Omega * I_{OH}) = 5.0V - 4.7V = 0.3V \quad at\ I_{OL} = 2.0mA$

Static Device Power *(P_{STR})*:

$$P_{STR} = SIDD * V_{DD} = 8.0mA * 5.0V = 40.0mW$$

Dynamic Power per Switching Receiver (P_{DYNR}):

$$P_{DYNR} = \left(C_{PD}\left(V_{DD}{}^2 * f\right)\right) + \left(C_L\left(V_{OH}(actual) - V_{OL}(actual)\right)^2 * f\right) =$$
$$\left(21.12pF\left(5.0V^2 * 40MHz\right)\right) + \left(20pF(5.0V - 0.3V)^2 * 40MHz\right) =$$
$$21.1mW + 17.7mW = 38.79mW$$

Resistive Output Load Power (P_{LOAD}):

$$P_{RLOAD} = \left[\left(P_{DCL} * V_{OL} * I_{OL}\right) + \left(P_{DCH} * \left(V_{DD} - V_{OH}\right) * \left|I_{OH}\right|\right)\right] =$$
$$\left[(0.5 * 0.3V * 2.0mA) + (0.5 * (5.0V - 5.0V) * 0.4mA)\right] = 0.3mW + 0 = 0.3mW$$

Total Device Power (P_{TOTALR}):

$$P_{TOTALRm} = P_{STR} + \left(N_O\left(P_{DYNR} + P_{RLOAD}\right)\right) =$$
$$= 40.0mW + (4(38.79mW + 0.3mW)) = 196.37mW$$

Quickly comparing this to Joule's Law (*P=I*V*):

4 switching outputs:

$$I = ((AIDD(slope)) * f * N_O) + SIDD = (0.304mA/MHz * 40MHz * 4) + 8.0mA = 56.64mA$$

$P = I * V = 56.64mA * 5.0V = 283.2mW$ for 4 outputs switching

If example 5 were recalculated using a C_L of *40pF*, a result of 267.06mW is obtained. Therefore, the C_{PD} form of the power calculation is within 6% of the Joule's Law form.

5.0 Conclusion

This application note empowers the designer to more accurately determine the power dissipation of Aeroflex's LVDS products as implemented in the user's application. The calculations described in the above sections employ application specific variables such as load capacitance, frequency, DC loading, etc that contribute to overall power dissipation. With accurate power dissipation improved power supply selection and thermal management schemes can be designed.

6.0 Additional Comments

Data contained in this application note is NOT GUARANTEED. The data is intended to provide system designers with better estimate of LVDS driver and receiver power dissipation.

To optimize power conservation tie unused driver inputs either high (V_{DD}) or low (V_{SS}), and leave unused outputs unconnected (no termination resistor connected, R_T).

Leave unused receiver inputs floating, the unused input pins should be floated near the pin on the receiver device. There is a fail safe mode on the Aeroflex LVDS receivers that force the outputs to a high state. Unused receiver inputs should not be connected to noise sources. Do not connect unused receiver input pins to a floating cable or trace because they will act as a noise antenna. Unused receiver outputs should be left unconnected to further power conservation.