Single Event Upset Design Techniques for UTMC's RadHard MSI Logic Family

Overview

A Single Event Upset (SEU) is the result of an ion transitioning through a semiconductor structure and depositing charge on a critical circuit node within that structure. In a CMOS logic circuit, the deposited charge can switch the logic state of sequential or combinatorial circuitry (i.e., upset the circuit). SEUs at the system or circuit design level can be considered noise in the system or circuit. To mitigate the effects of the noise, circuit designers can use various circuit design techniques. As a leader in the development of radiation-hardened products, United Technologies Microelectronics Center (UTMC) produces circuits to withstand the effects of charged particles (i.e., ions).

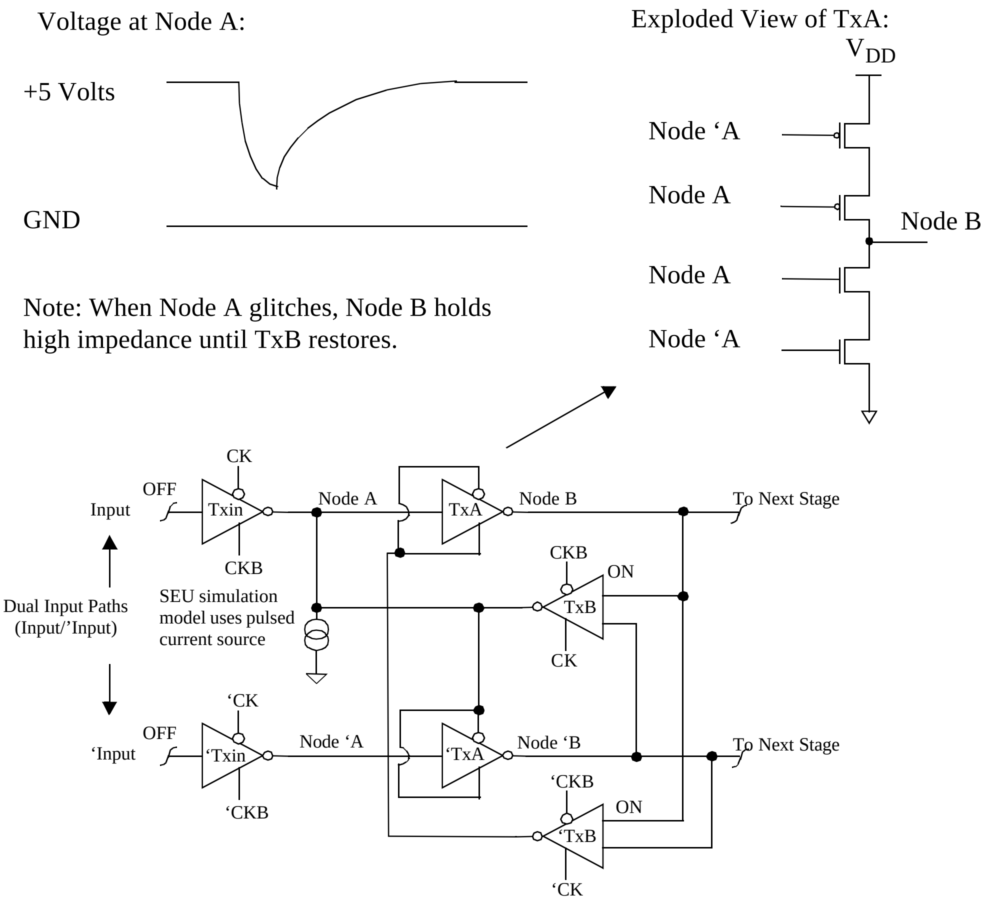
Typical SEU hardening techniques include: the addition of cross-coupled resistors or capacitors in storage cells, increased drive capacity on sensitive nodes, increased sensitive node capacitance, and dual circuit paths. The addition of cross-coupled resistors and capacitors in a storage cells slows the cell's ability to latch data. Increasing sensitive node drive capacity allows the node to quickly remove the charge deposited by the ion strike. Larger sensitive node capacitance requires more charge to upset the node, thus increasing the circuits immunity to some ions. Parallel circuits allow for the implementation of simple or complex voting schemes to reduce the noise injected by ion strikes. In all cases, the SEU hardening technique increases the physical area to implement the circuit.

The goal of UTMC's Rad-Hard MSI Logic Family development was to design a SEU hard family of products on bulk semiconductor material (i.e., 1.2μm CMOS, designated UTER) by utilizing a combination of hardening design techniques. Since the functionality of the family requires small physical areas, multiple hardening techniques were employed with little impact to the die size and no change in functionality. The primary technique utilized dual paths or redundant circuitry within the product.

Storage Cells

The primary SEU problem with storage cells lies in the feedback path. Amplification and feedback of noise (i.e., charge) on a critical node in the storage cell can permanently change a cell's logic state. To desensitize the storage cells of Rad-Hard MSI logic products, a dual or redundant path architecture was used. Figure 1 illustrates the design of a storage cell with dual circuitry. The SEU event is simulated with a pulsed current source representing noise. In Figure 1, Node A is in a storage state with the input gated inverter TXIN "off" and gated inverter TxB feeding back or "on". When Node A glitches, due to noise, TxA enters the high impedance state due to the "anding" of the inputs from parallel nodes A and 'A. To have a logic state change propagate to the outputs both Nodes A and 'A must enter the same state. If Node A and 'A do not enter the same state the output transitions to the high impedance state holding the previous state. As the SEU event passes, feedback inverter TxB restores Node A to the original value.

Figure 1. Dual Path Storage Cell



Note: When Node A glitches, Node B holds high impedance until TxB restores.

SEU simulation model uses pulsed current source

Storage Cell Testing

UTMC performed SEU immunity testing of hardened storage cells utilizing a dual-path architecture at Brookhaven National Laboratory on December 9, 1993. The testing was in conjunction with UTMC’s 1.2μm CMOS triple-layer metal process qualification. Table 1 lists data obtained from the test. The table lists saturated cross section versus Linear Energy Transfer (LET) for representative storage cells: flip-flop cell, dual-path “hard” flip-flop cell, and a static memory cell. The test device consisted of three circuits: 1024 bit array of “hard” flip-flops, 4096 bit array of D-type flip-flops, and a 8192 bit static memory array. Test circuits include all three storage cells on a single device with control logic to facilitate testing.

Figure 2 graphically illustrates the test results. Normalizing the data to account for the number of storage bits, the SRAM cell and D flip-flop performed similarly. Both the SRAM and D flip-flop exhibited saturated cross sections around 1.0E-6 cm^2/bit, while the “hard” flip-flop exhibited a cross section around 1.0E-9 cm^2/bit. Note the LET values of the SRAM and D flip-flop begin to roll-off at a LET of 40 MeV-cm^2/mg while the “first-event” observed within a “hard” flip-flop did not occur until a LET of 80MeV-cm^2/mg. Overall, the “hard” flip-flop tested superior (2x) for both LET and saturated cross section (2.5 orders of magnitude) than the reasonably hard SEU resistant UTER storage cells.

Depending upon the environment, varying upset rates can be projected for the Rad-Hard MSI Family. The error rate projections depend upon the saturated cross sections, LET value, shielding, and ambient atmosphere conditions (i.e., orbit). Please reference UTMC’s Radiation-Hardened CMOS Technical Description (October 1992) for examples of obtaining error rates.

While the SRAM cell and the D flip-flop cell exhibited well behaved cross section versus LET curves, the “hard” flip-flop cell exhibited fluctuation around its LET threshold. No upsets were recorded below 80 MeV-cm^2/Mg for the “hard” flip-flop; however; not all particle strikes at 80 MeV-cm^2/mg resulted in upsets. The best explanation for the intermittent upset threshold of the ”hard” flip-flop was due to control line glitches. The control line upset results in write upset as opposed to storage cell upset. Inspection of the control logic circuitry determined a resistive stack in the write path. In the design of the Rad-Hard MSI Logic Family, special care was taken to eliminate control line upset to insure the overall family hardness.

Table 1: SEU Test Data: Storage Cells 1.2μm CMOS (UTER)

LET (MeV-cm^2/mg)	“Hard” Flip-Flop (cm^2/bit)	D-Type Flip-Flop (cm^2/bit)	SRAM Cell (cm^2/bit)
125.0			1.38E-06
120.0	2.92E-09		1.60E-06
120.0	2.83E-09		
115.0		1.16E-06	
110.0			1.51E-06
100.0	5.36E-09		1.55E-06
100.0	2.24E-09		
100.0	9.75E-11		
95.0		1.07E-06	
90.0			1.37E-06
80.0	2.14E-09		1.25E-06
80.0	9.77E-16[1]		
80.0	9.77E-16[1]		
80.0	9.77E-16[1]		
75.0		4.79E-07	

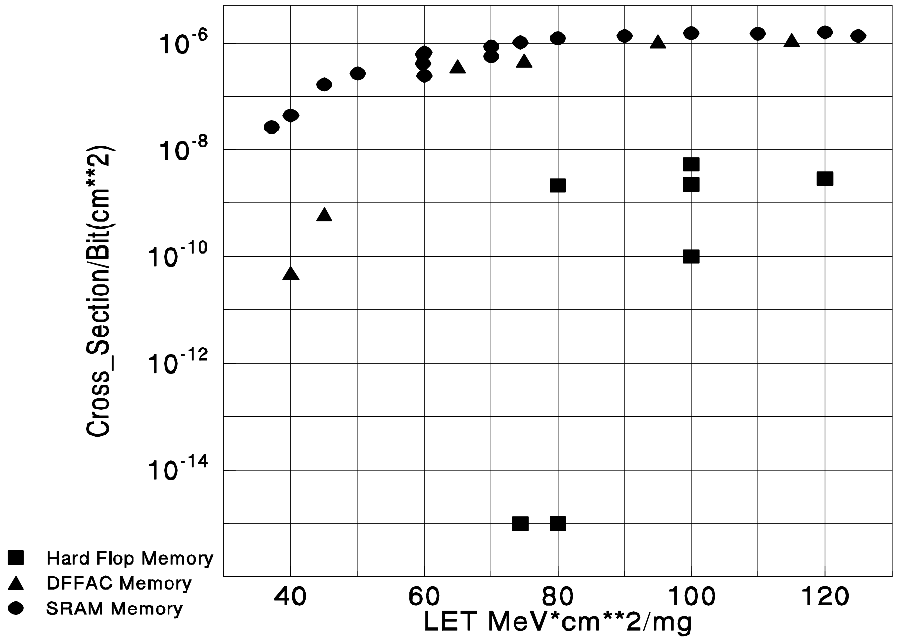
Table 1: SEU Test Data: Storage Cells 1.2µm CMOS (UTER)

LET (MeV-cm^2/mg)	"Hard" Flip-Flop (cm^2/bit)	D-Type Flip-Flop (cm^2/bit)	SRAM Cell (cm^2/bit)
74.4			1.04E-06
74.4	9.77E-16[1]		
70.0			8.70E-7
70.0			5.67E-07
65.0		3.69E-07	
60.0			6.63E-07
60.0			2.48E-07
59.8			6.19E-07
59.8			4.11E-07
50.0			2.72E-07
45.0		6.25E-10	1.69E-07
40.0		4.87E-11	4.42E-08
37.2			2.69E-08

Note:
1. No measurable upset was assigned a value of 9.77E-16

Figure 2. SEU Storage Cell Test Results

(SRAM,DFFAC, & Hard Flop Cells)



Note: <1E-14 Represents Zero/No Upsets

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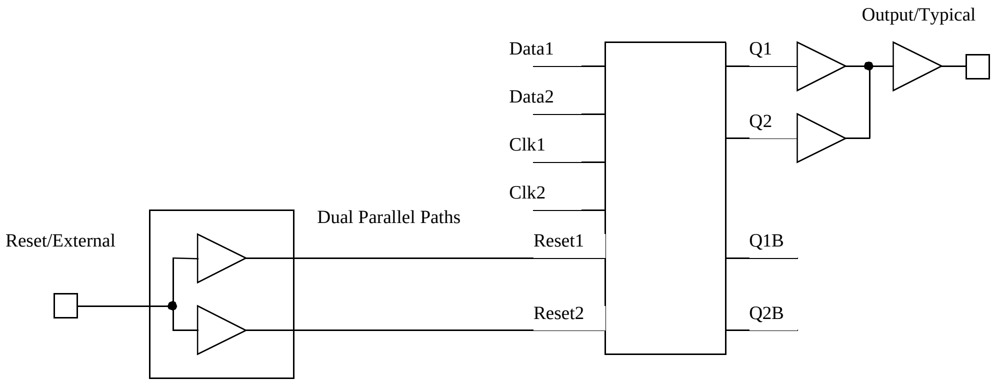
Combinatorial Paths/Set/Resets

UTMC exercised special care in the design of all combinatorial and control circuitry for the Rad-Hard MSI Logic Family. Figure 3 shows the basic methodology employed in designing the combinatorial/control logic. At the input pad, the signal paths were immediately split after the input protection devices and routed in parallel on the device. Figure 3 also illustrates dual outputs from a storage cell. At the final output buffer the dual-paths recombine. Recombination was via a minimum stack “OR”, or by coming directly from the hard storage cell output. The resulting circuitry limits the device’s ability to glitch below their intended operating threshold.

Figure 3. Typical Rad-Hard MSI Combinatorial Paths(s)
(Illustrating External to Internal Reset Path and Internal to External Path)



Summary

UTMC utilized years of experience in developing the Rad-Hard MSI Logic Product Family. In addition to superb SEU immunity, the Rad-Hard MSI device family will not latch-up when struck by heavy ions or exposed to gamma radiation. The device family will operate per the data sheet when exposed to 1Mrads (Si). The entire family is Defense Electronic Supply Center (DESC) certified and is available off-the shelf.