REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outlines U, T, and M. Add all radiation requirements. -tmh	00-02-08	Monica L. Poelking
B	Add 3.3 V option throughout document. - tmh	00-03-30	Monica L. Poelking
C	Add dose rate note 5/ to paragraph 1.5. Add dose rate requirement to paragraph 3.3. - tmh	00-06-13	Monica L. Poelking
D	Add appendix A die requirements and case outline N. -tmh	01-02-02	Thomas M. Hess
E	Add case outline 4 and 5. Update boileplate. -phn	01-05-03	Thomas M. Hess
F	Correct footnote 1/ in 1.2.2 Device type. Add footnote 7/ to 1.3 Absolute maximum ratings. Remove OSC buffer test in table I. -phn	02-05-22	Thomas M. Hess
G	Add Schmitt trigger for TTL test, in table I. Update boilerplate. -phn	05-03-03	Thomas M. Hess
H	Add V_{DDC} to Cold spare inputs-"On" in table I. – phn	05-04-04	Thomas M. Hess
J	Correct pin labels in case 4, figure 1 – phn	05-11-01	Thomas M. Hess
K	Device type 14 and 15 are no longer available. Updated "Radiation features", in section 1.5. - phn	10-07-12	Thomas M. Hess
L	Add device type 02 to the appendix A. - phn	10-11-23	Thomas M. Hess

REV																				
SHEET																				
REV	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32		

REV STATUS	REV	L	L	L	L	L	L	L	L	L	L	L	L	L
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
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DRAWING APPROVAL DATE
99-06-22

REVISION LEVEL
L

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, GATE ARRAY, RADIATION HARDENED, MONOLITHIC SILICON

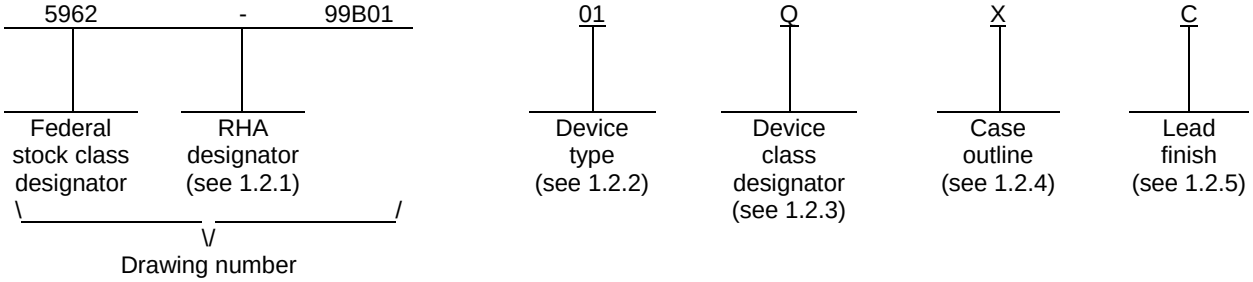
SIZE	CAGE CODE	
A	**67268**	**5962-99B01**

SHEET 1 OF 32

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Signal I/O 2/	Power & Ground Pads 3/
01	06MRA010	10,000 gates available	58	6
02	06MRA025	25,000 gates available	192	48
03	06MRA050	50,000 gates available	192	48
04	06MRA075	75,000 gates available	308	76
05	06MRA100	100,000 gates available	308	76
06	06MRA150	150,000 gates available	308	76
07	06MRA200	200,000 gates available	432	96
08	06MRA250	250,000 gates available	432	96
09	06MRA300	300,000 gates available	432	96
10	06MRA350	350,000 gates available	432	96
11	06MRA400	400,000 gates available	544	144
12	06MRA450	450,000 gates available	544	144
13	06MRA500	500,000 gates available	544	144
14	06MRA550 4/	550,000 gates available	544	144
15	06MRA600 4/	600,000 gates available	544	144

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1/ These devices are capable of being configured and support dual voltage: 3.3 V core / 3.3 V and/or 5 V bus, 5 V core/5 V bus. The supply voltage range shall be specified in the AID.
2/ Includes 5 pins that may or may not be reserved for JTAG boundary scan.
3/ Reserved for dedicated V_{DD}/V_{SS} and V_{DDQ}/V_{SSQ}.
4/ No longer available from an approved source of supply.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CQCC2-F172	172	Quad leaded chip carrier
Y	CQCC2-F196	196	Quad leaded chip carrier
Z	CQCC1-F132	132	Unformed-lead chip carrier Non-conductive tiebar
U	See figure 1	240	Ceramic flatpack
T	See figure 1	304	Ceramic flatpack
M	CQCC1-F172	172	Unformed leaded chip carrier
N	CQCC1-F84	84	Ceramic Flatpack
4	See figure 1	256	Ceramic Flatpack
5	See figure 1	352	Ceramic Flatpack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 5/

DC supply voltage (V_{DD})
- 5.0 Volt configuration ..... -0.3 V to 6.0 V
- 3.3 Volt configuration ..... -0.3 V to 3.9 V

Voltage on any pin ($V_{I/O}$) 6/
- 5.0 Volt configuration ..... -0.3 V to V_{DD} + 0.3 V
- 3.3 Volt configuration ..... -0.3 V to V_{DD} + 0.3 V

Storage temperature (T_{STG}) ..... -65°C to +150°C
Maximum junction temperature (T_J) ..... +175°C
Latchup immunity (I_{LU}) ..... ±150 mA
DC input current (I_I) ..... ±10 mA
Lead Temperature (soldering 5 sec) ..... +300°C

1.4 Recommended operating conditions.

Positive supply voltage (V_{DD})
- 5.0 Volt configuration ..... 4.5 V to 5.5 V
- 3.3 Volt configuration ..... 3.0 V to 3.6 V

Case temperature range (T_C) ..... -55°C to +125°C
DC input voltage (V_{IN}) ..... 0 V to V_{DD}

1.5 Radiation features.

Total dose:
- For device 01 through 04 (Dose rate = 50 – 300 Rad(Si)/s) ..... $\geq 3 \times 10^5$ Rads (Si) 7/
- For device 05 through 15 (Dose rate = 50 – 300 Rad(Si)/s) ..... $\geq 1 \times 10^5$ Rads (Si) 7/

Single event phenomenon (SEP) effective
- LET, no upset 8/
- LET, no latchup ..... $\geq$ 109 MeV-cm^2/mg

Dose rate upset (20 ns pulse) ..... 4.4×10^8 Rad(Si)/s at 4.5 V_{DD} 9/
Dose rate latchup ..... $> 3.8 \times 10^{11}$ Rad(Si)/s 9/
Dose rate survivability ..... $> 3.8 \times 10^{11}$ Rad(Si)/s 9/
Neutron irradiated ..... 1.0×10^{14} neuron/cm^2

1.6 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) ..... as specified in the AID

5/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
6/ For cold spare mode ($V_{DD} = V_{SS}$), $V_{I/O}$ would be ± 0.3 V to maximum recommended operating condition.
7/ The dose rate shall be 50 – 300 Rad(Si)/s unless otherwise specified in the AID.
8/ When characterized as a result of the procuring activities request, the condition will be specified.
9/ Applicable to ON Semi Fab 9 fabricated material

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.
MIL-PRF-123 - Capacitors, Fixed, Ceramic Dielectric, (Temperature Stable and General Purpose), High Reliability, General Specification for

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non Government publications. The following document(s) for a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and as specified in figure 1.

3.3 AID requirements. All AIDs written against this SMD shall be sent to DLA Land and Maritime -VA. The following items shall be provided to the device manufacturer by the customer as part of an AID.

3.3.1 Terminal connections and pin assignments.

3.3.2 Package type (see 1.2.4).

3.3.3 Functional block diagram (or equivalent HDL behavioral description).

3.3.4 Functional description terms and symbols.

3.3.5 Logic diagram (or equivalent structural HDL description or mutually agreed to net list).

3.3.6 Pin function description.

3.3.7 Design tape # or Design document name (i.e., net list).

3.3.8 Design functional tape # or name.

3.3.9 Test functional tape # or name.

3.3.10 Timing diagram(s).

3.3.11 Fault coverage measurement of manufacturing logic tests.

3.3.12 Burn-in circuit.

3.3.13 ESD class and voltage.

3.3.14 Device electrical performance characteristics (additions to Table I). Device electrical performance characteristics shall include dc parametric, functional, ac parameters and any other data which would be considered required by a design engineer. All electrical performance characteristics apply over the full recommended ambient operating temperature range and specified test load conditions.

3.3.15 Maximum power dissipation. Maximum power dissipation shall be in accordance with the application specific design.

3.3.16 Supply voltage range. The supply voltage range shall be as specified in the AID.

3.3.17 Dose rate. The dose rate shall be 50 – 300 Rad(Si)/s depending on total dose requirement; unless otherwise specified in the AID.

3.4 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A. The AID number shall be added to the marking by the manufacturer.

3.6.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.10 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime 's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ V_{DD} = 5.0 V ± 10% V_{DDC} = 5.0/3.3 V ± 10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low-level input voltage 3/							
TTL inputs	V_{IL}	V_{DD} = 4.5 V and 5.5 V	1, 2, 3	All		0.8	V
CMOS inputs						$0.3V_{DD}$	
High-level input voltage 3/							
TTL inputs	V_{IH}	V_{DD} = 4.5 V and 5.5 V	1, 2, 3	All	2.2		V
CMOS inputs					$0.7V_{DD}$		
Schmitt Trigger, positive going threshold 3/	V_T+	V_{DD} = 4.5 V and 5.5 V	1, 2, 3	All			
TTL						2.4	V
CMOS						$0.7V_{DD}$	
Schmitt Trigger, negative going threshold 3/	V_T-	V_{DD} = 4.5 V and 5.5 V	1, 2, 3	All			
TTL					0.9		V
CMOS					$0.3V_{DD}$		
Schmitt Trigger, typical range of hysterisis 4/	V_H		1, 2, 3	All			
TTL					0.4		V
CMOS					0.6		
Input leakage current	I_{IN}	V_{DD} = 5.5 V					
TTL, CMOS and Schmitt inputs		$V_{IN} = V_{DD}$ and V_{SS}	1, 2, 3	All	-1	1	µA
Inputs with pull-down resistors		$V_{IN} = V_{DD}$			20	225	
Inputs with pull-down resistors		$V_{IN} = V_{SS}$			-5	5	
Inputs with pull-up resistors		$V_{IN} = V_{SS}$			-225	-20	
Inputs with pull-up resistors		$V_{IN} = V_{DD}$			-5	5	
Cold spare inputs – "Off"		V_{IN} = 0 to 5.5 V			-5	5	
Cold spare inputs – "On"		$V_{DDC} = V_{DD} = V_{SS}$ = 0 V V_{IN} = 0 V and 5.5 V			-5	5	
Low-level output voltage	V_{OL}	V_{DD} = 4.5 V	1, 2, 3	All			
TTL 2.0 mA buffer		I_{OL} = 2.0 mA				0.4	V
TTL 4.0 mA buffer		I_{OL} = 4.0 mA				0.4	
TTL 8.0 mA buffer		I_{OL} = 8.0 mA				0.4	
TTL12.0 mA buffer		I_{OL} = 12.0 mA				0.4	
CMOS outputs		I_{OL} = 1.0 µA				0.05	
CMOS outputs (Optional)		I_{OL} = 100.0 µA				0.25	
CMOS outputs (Cold spare)		I_{OL} = 100.0 µA				0.25	
High-level output voltage	V_{OH}	V_{DD} = 4.5 V	1, 2, 3	All			
TTL 2.0 mA buffer		I_{OH} = -2.0 mA			2.4		V
TTL 4.0 mA buffer		I_{OH} = -4.0 mA			2.4		
TTL 8.0 mA buffer		I_{OH} = -8.0 mA			2.4		
TTL12.0 mA buffer		I_{OH} = -12.0 mA			2.4		
CMOS outputs		I_{OH} = -1.0 µA			V_{DD} - 0.05		
CMOS outputs (Optional)		I_{OH} = -100.0 µA			V_{DD} - 0.35		
CMOS outputs (Cold spare)		I_{OH} = -100.0 µA			V_{DD} - 0.35		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $V_{DD} = 5.0\ V \pm 10\%$ $V_{DDC} = 5.0/3.3\ V \pm 10\%$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Three-state output leakage current	I_{OZ}	$V_{DD} = 5.5\ V$		1, 2, 3	All			µA
TTL 2.0 mA buffer						-5	5	
TTL 4.0 mA buffer						-10	10	
TTL 8.0 mA buffer						-20	20	
TTL12.0 mA buffer						-30	30	
Cold spare inputs – "Off"		$V_O = 0\ V$ and $5.5\ V$				-5	-5	
Cold spare inputs – "On"		$V_{DDC} = V_{DD} = V_{SS} = 0\ V$ $V_O = 0\ V$ and $5.5\ V$				-5	-5	
Short-circuit output current 4/ 5/	I_{OS}	$V_O = 0\ V$ and $5.5\ V$		1, 2, 3	All			mA
TTL 2.0 mA buffer						-50	50	
TTL 4.0 mA buffer						-100	100	
TTL 8.0 mA buffer						-200	200	
TTL12.0 mA buffer						-300	300	
Quiescent supply current 6/	I_{DDQ}	$V_{DD} = 5.5\ V$ 200K gates		1,3	All		50	µA
		400K gates					100	
		600K gates					150	
		$V_{DD} = 5.5\ V$ 200K gates		2	All		1	
		400K gates					2	mA
		600K gates					3	
		$V_{DD} = 5.5\ V$ 200K gates		1	All		4	
		400K gates	M, D, P, L, R				8	mA
		600K gates					12	
Input capacitance 7/	C_{IN}			4	All		23	pF
Output capacitance 7/								
TTL 2.0 mA buffer	C_{OUT}			4	All		22	pF
TTL 4.0 mA buffer							26	
TTL 8.0 mA buffer							26	
TTL12.0 mA buffer							26	
Bidirect I/O capacitance 7/								
TTL 4.0 mA buffer	C_{IO}			4	All		24	pF
TTL 8.0 mA buffer							26	
TTL12.0 mA buffer							26	

See notes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ V_{DD} = 3.3 V ± 10% V_{DDC} = 3.3 V ± 10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low-level input voltage CMOS inputs 3/	V_{IL}	V_{DD} = 3.0 V and 3.6 V	1, 2, 3	All		$0.3V_{DD}$	V
High-level input voltage CMOS inputs 3/	V_{IH}	V_{DD} = 3.0 V and 3.6 V	1, 2, 3	All	$0.7V_{DD}$		V
Schmitt Trigger, positive going threshold 3/	V_T+	V_{DD} = 3.0 V and 3.6 V	1, 2, 3	All		$0.7V_{DD}$	V
Schmitt Trigger, negative going threshold 3/	V_T-	V_{DD} = 3.0 V and 3.6 V	1, 2, 3	All	$0.3V_{DD}$		V
Schmitt Trigger, typical range of hysterisis 4/	V_H		1, 2, 3	All	0.6		V
Input leakage current		V_{DD} = 3.6 V	1, 2, 3	All			
CMOS and Schmitt inputs		$V_{IN} = V_{DD}$ and V_{SS}			-1	1	µA
Inputs with pull-down resistors		$V_{IN} = V_{DD}$			10	225	
Inputs with pull-down resistors	I_{IN}	$V_{IN} = V_{SS}$			-5	5	
Inputs with pull-up resistors		$V_{IN} = V_{SS}$			-225	-10	
Inputs with pull-up resistors		$V_{IN} = V_{DD}$			-5	5	
Cold spare inputs – “Off”		V_{IN} = 0 to 3.6 V			-5	5	
Cold spare inputs – “On”		$V_{DDC} = V_{DD} = V_{SS}$ = 0 V V_{IN} = 0 V and 3.6 V.			-5	5	
Low-level output voltage	V_{OL}		1, 2, 3	All			
CMOS outputs		I_{OL} = 1.0 µA				0.05	V
CMOS outputs (Optional)		I_{OL} = 100.0 µA				0.25	
CMOS outputs (cold spare)		I_{OL} = 100.0 µA				0.25	
High-level output voltage	V_{OH}		1, 2, 3	All			
CMOS outputs		I_{OH} = -1.0 µA			V_{DD} - 0.05		V
CMOS outputs (Optional)		I_{OH} = -100.0 µA			V_{DD} - 0.35		
CMOS outputs(cold spare)		I_{OH} = -100.0 µA			V_{DD} - 0.35		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ V_{DD} = 3.3 V ± 10% V_{DDC} = 3.3 V ± 10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Three-state output leakage current CMOS Cold spare inputs – "Off" Cold spare inputs – "On"	I_{OZ}	V_{DD} = 3.6 V $V_O = V_{DD}$ and V_{SS} V_O = 0 V and 3.6 V $V_{DDC} = V_{DD} = V_{SS}$ = 0 V $V_{IN} = V_{DD}$ or V_{SS}	1, 2, 3	All	-20 -5 -5	20 5 5	µA
Short-circuit output current 4/ 5/ CMOS	I_{OS}	V_O = 0 V and 3.6 V	1, 2, 3	All	-200	200	mA
Quiescent supply current 6/	I_{DDQ}	V_{DD} = 3.6 V 200K gates 400K gates 600K gates	1,3	All		50 100 150	µA
		V_{DD} = 3.6 V 200K gates 400K gates 600K gates	2			1 2 3	mA
		V_{DD} = 3.6 V 200K gates 400K gates 600K gates M, D, P, L, R	1	All		4 8 12	mA
Input capacitance 7/	C_{IN}		4	All		23	pF
Output capacitance 7/ CMOS	C_{OUT}		4	All		26	pF
Bidirect I/O capacitance 7/ CMOS	C_{IO}		4	All		26	pF

Notes:

1/ These devices are capable of being configured and support dual voltage: 3 V core/3.3 V bus or 5 V core/5 V bus. The supply voltage range shall be specified in the AID.

2/ Devices supplied to this drawing will meet all levels M, D, P, L and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25 C.

3/ Functional tests are conducted in accordance with MIL-STD-883 with the following input conditions: $V_{IH} = V_{IH}(min)$ + 20%, - 0%; $V_{IL} - V_{IL}(max)$ +0%, -50%, as specified herein for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.

4/ Supplied as a design limit but not guaranteed or tested.

5/ Not more than one output may be shorted at a time for maximum duration of one second.

6/ All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

7/ Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1 MHz @ 0 V and a signal amplitude of ≤ 50 mV RMS.

TABLE IB. SEP test limits . 1/ 2/

Device Type	T_A = Temperature ±10°C	SEU BIAS, V_{CC} = 4.5 V		Bias for latch-up test V_{CC} = 5.5 V, no latch-up LET = 3/
		Effective LET no upsets [MEV – cm^2/mg]	Maximum device cross section (μm^2) (LET = 120)	
All	3/	4/	4/	≥ 109 Mev – mg/cm^2

NOTE: Devices that contain cross coupled resistance must be tested at the maximum rated T_A.
1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature T_A = +125°C.
4/ When characterized as a result of the procuring activities request, this parameter will be specified.

TABLE IC. Biasing for TID exposure.

OPEN	V_{DD} = 5.5 V	GROUND
A14, A15, A16, A17, B2, B14, B15, B16, B18, C2, C3, C8, C9, C14, C15, D2, D3, D7, D8, D9, D13, D14, D18, E1, E2, E5, E6, E9, D6, D9, E12, E13, F2, F3, F5, F17, G3, G4, G19, H1, H3, H4, H5, H19, J17, J18, J19, K17, K18, L16, L17, L18, L19, M16, M17, M18, M19, N5, N16, N17, N18, N19, N20, P4, P16, P17, P18, P19, P20, R4, R5, R16, R17, R18, R19, R20, T2, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U7, U8, U9, U10, U11, U13, U14, U15, U16, U17, U18, U19, U20, V8, V9, V10, V11, V12, V14, V15, V16, V17, V18, V19, W3, W4, W5, W6, W7, W8, W9, W10, W11, W12, W14, W15, W16, W17, W18, W19, X4, X5, X6 ,X7, X13, X14, X15, X16	A3, A5, A7, A9, A11, A13, A18, A20, B1, B3, B5, B7, B8, B10, B13, C4, C6, C10, C13, C17, C19, C20, D1, D5, D6, D15, D16, D17, D20, E4, E7, E10, E11, E15, E17, E20, F1, F16, F19, G2, G16, G18, H2, H17, J2, J4, J16, J20,, K1, K3, K5, K19, L3, L4, L20, M1, M2, M4, N2, N4, P1, P3, R1, R2, T1, T4, T6, T7, U2, U5, U12, V3, V4, V5, V7, V20, W1, W2, X2, X8, X10, X12, X18, X20	A2, A4, A6, A8, A10, A12, A19, B4, B6, B9, B11, B12, B17, B19, B20, C1, C5, C7, C11, C12, C16, C18, D4, D10, D11, D12, D19, E3, E8, E14, E16, E18, E19, F4, F18, F20, G1, G5, G17, G20, H16, H18, H20, J1, J3, J5, K2, K4, K16, K20, L1, L2, L5, M3, M5, M20, N1, N3, P2, P5, R3, T3, T5, U1, U3, U4, U6, V1, V2, V6, V13, W13, W20, X1, X3, X9, X11, X17, X19

1/ The device manufacturer performs radiation testing using a 299 Pin grid array for the standard evaluation circuit.

Case U

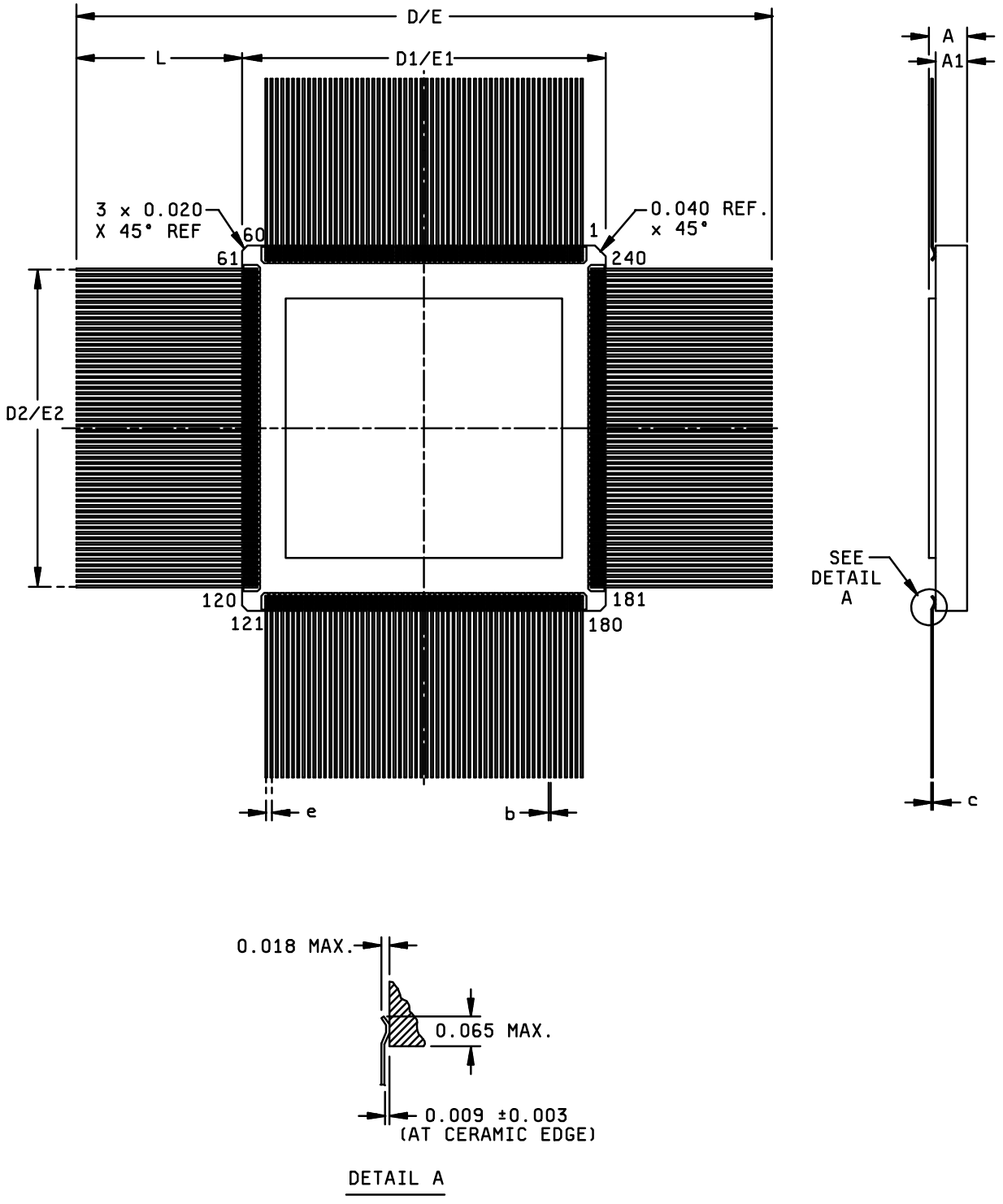


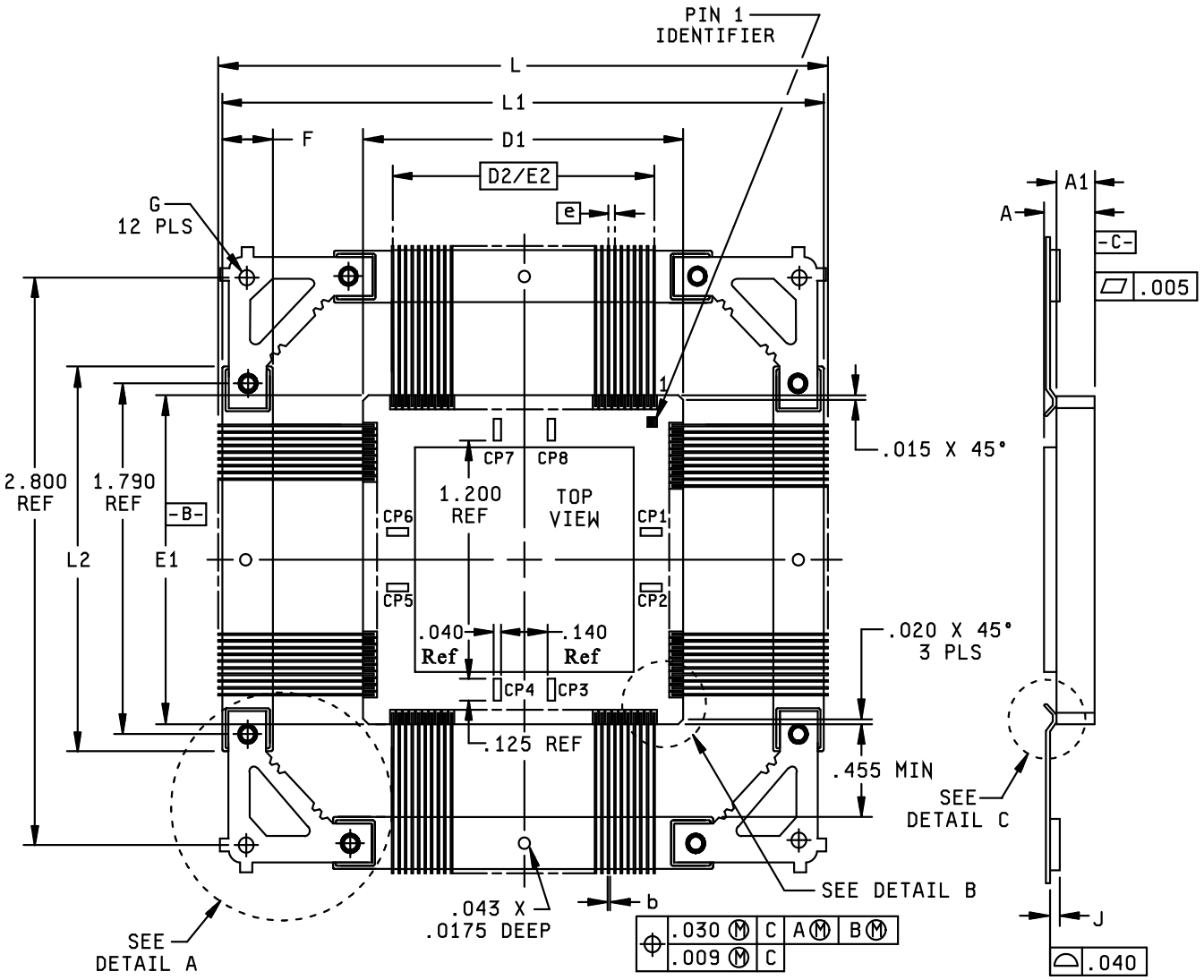
Figure 1. Case outline.

Case U

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.76		0.148
A1		3.25		0.128
b	0.152	0.254	0.006	0.010
c	0.102	0.203	0.004	0.008
D/E		77.22		3.040
D1/E1	33.68	34.34	1.326	1.352
D2/E2	29.5 BSC		1.1614 BSC	
e	0.50 BSC		0.020 BSC	
L	14.96		0.589	

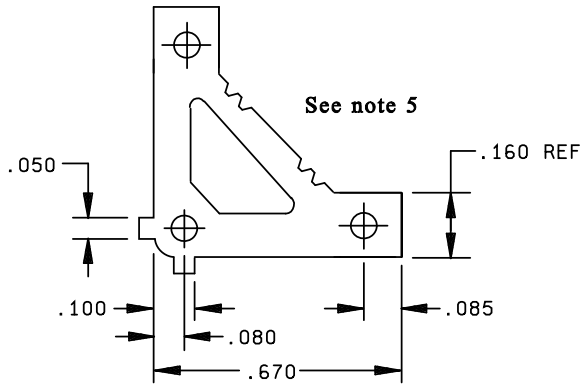
Figure 1. Case outline – Continued.

Case T

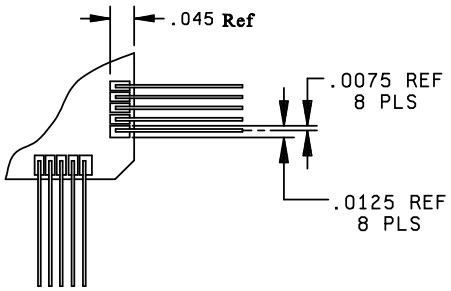


CP1	V_{DD}	CP5	V_{DD}
CP2	V_{SS}	CP6	V_{SS}
CP3	V_{DDQ}	CP7	V_{DDQ}
CP4	V_{SSQ}	CP8	V_{SSQ}

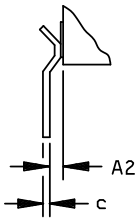
Figure 1. Case outline – Continued.



DETAIL A



DETAIL B



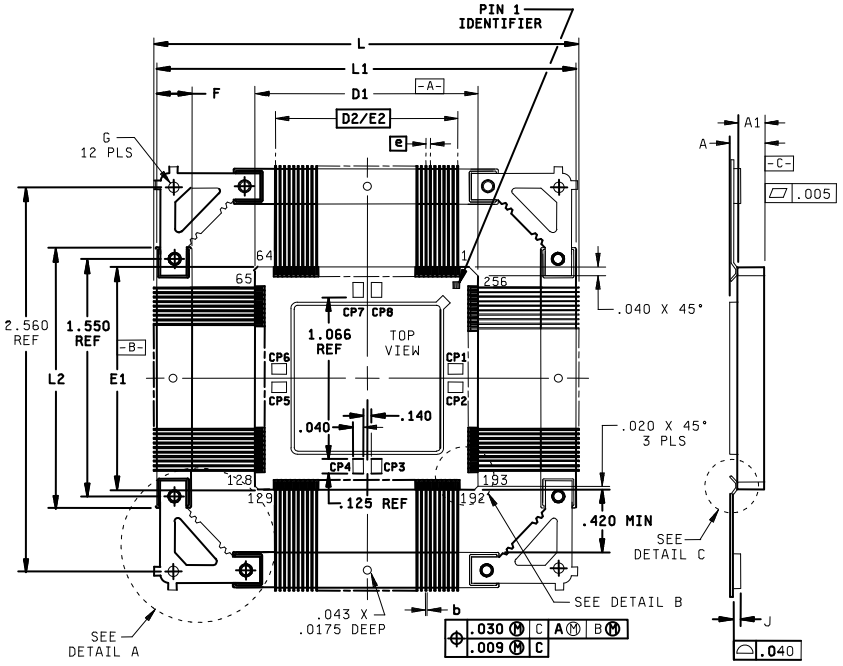
DETAIL C

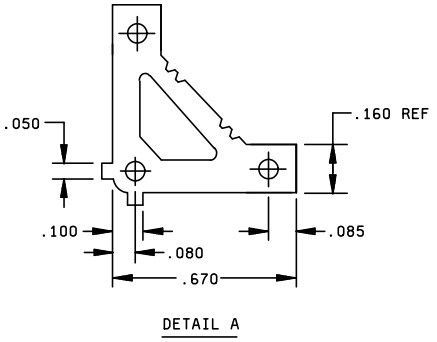
Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		3.302		0.130	e	0.508		0.020 BSC	
A1		2.667		0.105	F		5.080		0.200
A2	0.051	0.356	0.002	0.014	J	0.762	1.016	0.030	0.040
b	0.152	0.254	0.006	0.010	L		77.978		3.070
c	0.127	0.203	0.005	0.008	L1	75.946	76.454	2.990	3.010
D1/E1	41.529	42.291	1.635	1.665	L2		51.308		2.020
D2/E2	34.925 BSC		1.500 BSC						

Notes:

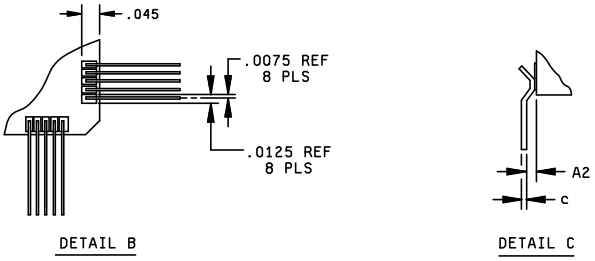
1. All exposed metalized areas are gold plated over nickel plating.
2. Capacitor mounting pads are dimensioned for an AVX/MIL-C-55681, P/N CDR05, 50 V 0.1 μf chip capacitor.
3. Capacitor mounting pads labeled V_{SS}, V_{DD}, V_{SSQ}, or V_{DDQ} are connected to their respective internal ground or power planes.
4. The lid is electrically connected to V_{SS}.
5. These areas may have notches and tabs different than shown.

Figure 1. Case outline – Continued.





DETAIL A



DETAIL B DETAIL C

Figure 1. Case outline – Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.302		0.130
A1		2.667		0.105
A2		0.356		0.014
b	0.152	0.254	0.006	0.010
c	0.127	0.203	0.005	0.008
D1/E1	36.703	37.465	1.445	1.475
D2/E2	32.004 BSC		1.260 BSC	
e	0.508		0.020 BSC	
F		5.080		0.200
J	0.762	1.016	0.030	0.040
L		72.898		2.870
L1	69.850	70.358	2.750	2.770
L2		45.212		1.780

CP1	VDD	CP3	VDDQ	CP5	VDD	CP7	VDDQ
CP2	VSS	CP4	VSSQ	CP6	VSS	CP8	VSSQ

Notes:
1. All exposed metalized areas are gold plated over nickel plating.
2. Capacitor mounting pads are dimensioned for an AVX/MIL-C-55681, P/N CDR05, 50 V 0.1 μf chip capacitor.
3. Capacitor mounting pads labeled V_{SS}, V_{DD}, V_{SSQ}, or V_{DDQ} are connected to their respective internal ground or power planes.
4. The lid is electrically connected to V_{SS}.
5. These areas may have notches and tabs different than shown.

Figure 1. Case outline – Continued.

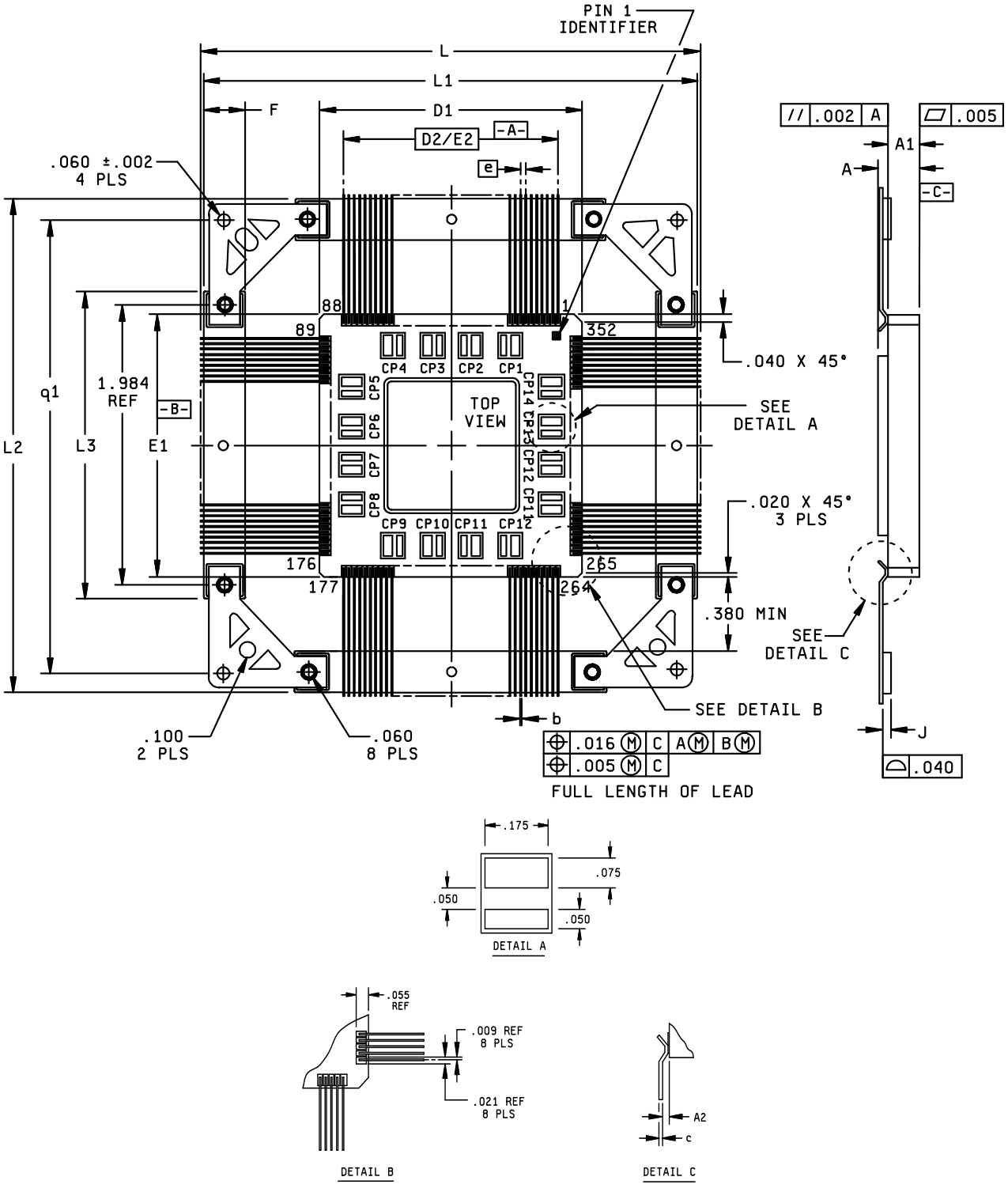


Figure 1. Case outline – Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.327		0.131
A1		3.251		0.128
A2		0.889		0.035
b	0.152	0.254	0.006	0.010
c	0.102	0.203	0.004	0.008
D1/E1	47.676	48.336	1.877	1.903
D2/E2	43.510 BSC		1.713 BSC	
e	0.483 BSC		0.019 BSC	
F		5.740		0.226
J	0.762	1.016	0.030	0.040
L		77.216		3.040
L1		75.387		2.968
L2	74.625	75.387	2.938	2.968
L3	55.677	56.947	2.192	2.242
q1		70.002		2.756

CP1	VSS	CP5	VSS	CP9	VSS	CP13	VSS
	VDD1		VDD1		VDD1		VDD1
CP2	VSS	CP6	VSS	CP10	VSS	CP14	VSS
	VDD2		VDD2		VDD2		VDD2
CP3	VSSQ	CP7	VSSQ	CP11	VSSQ	CP15	VSSQ
	VDDNCQ		VDDNCQ		VDDNCQ		VDDNCQ
CP4	VSSQ	CP8	VSSQ	CP12	VSSQ	CP16	VSSQ
	VDDCQ		VDDCQ		VDDCQ		VDDCQ

Notes:
1. All exposed metalized areas are gold plated over nickel plating.
2. Capacitor mounting pads are dimensioned for an AVX/MIL-C-55681, P/N CDR05, 50 V 0.1 μf chip capacitor.
3. Capacitor mounting pads labeled V_{SS}, V_{DD}, V_{SSQ}, or V_{DDQ} are connected to their respective internal ground or power planes.
4. The lid is electrically connected to V_{SS}.
5. These areas may have notches and tabs different than shown.

Figure 1. Case outline – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class Q and V, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device as described in the AID.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for initial qualification and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND. Capacitance testing shall be performed on three devices per Method 3012. A minimum of four pins per device shall be tested. Tested pins shall be selected based on engineering analysis of the package interconnect drawing to determine which pins will have the highest capacitance. The sample sizes may be increased based on engineering judgement, but shall not be decreased.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/
Group A test requirements (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/
Group D end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25 °C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. Neutron testing shall be performed in accordance with test method 1017 of MIL-STD-883 and herein (See 1.4). All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I, for the subgroups specified in Table IIA herein at TA = +25°C ± 5°C after an exposure of 2×10^{12} neutrons/cm^2 (minimum).

4.4.4.3 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (See 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (See 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.5). SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be as specified in Table IB SEP test limits.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0547.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

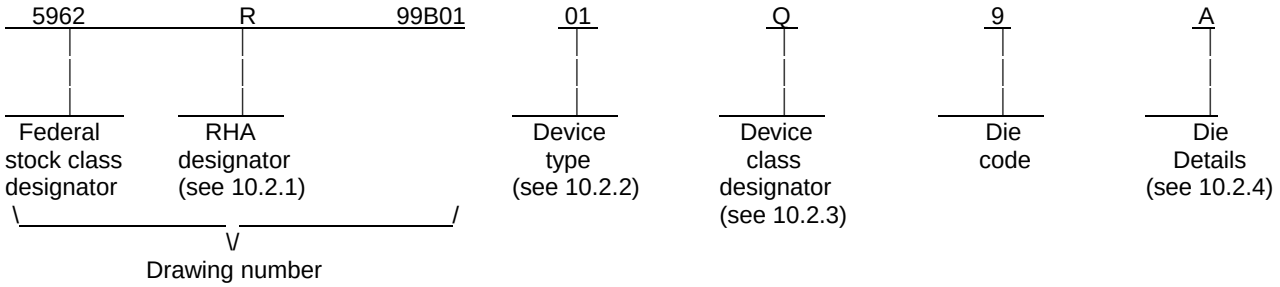
d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	06MRA010	Gate Array 10,000 gates available
02	06MRA025	Gate Array 25,000 gates available

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4. Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1
02	A-2

10.2.4.2. Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1
02	A-2

10.2.4.3. Interface materials.

Die type	Figure number
01	A-1
02	A-2

10.2.4.4. Assembly related information.

Die type	Figure number
01	A-1
02	A-2

10.3. Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, and handbooks. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

20.2. Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacture's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figure A-1 or A-2.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figure A-1 or A-2.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figure A-1 or A-2.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figure A-1 or A-2.

30.2.5 Truth table(s). The truth table(s) shall be as defined within paragraph 3.2.3. of the body of this document.

30.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.4. of the body of this document.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or 'Q' as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. VERIFICATION

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined within H.3.2.3 as approved by the manufacturers TRB and the Qualifying activity.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1., 4.4.4.2, 4.4.4.3, 4.4.4.4 and 4.4.4.5.

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60 NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

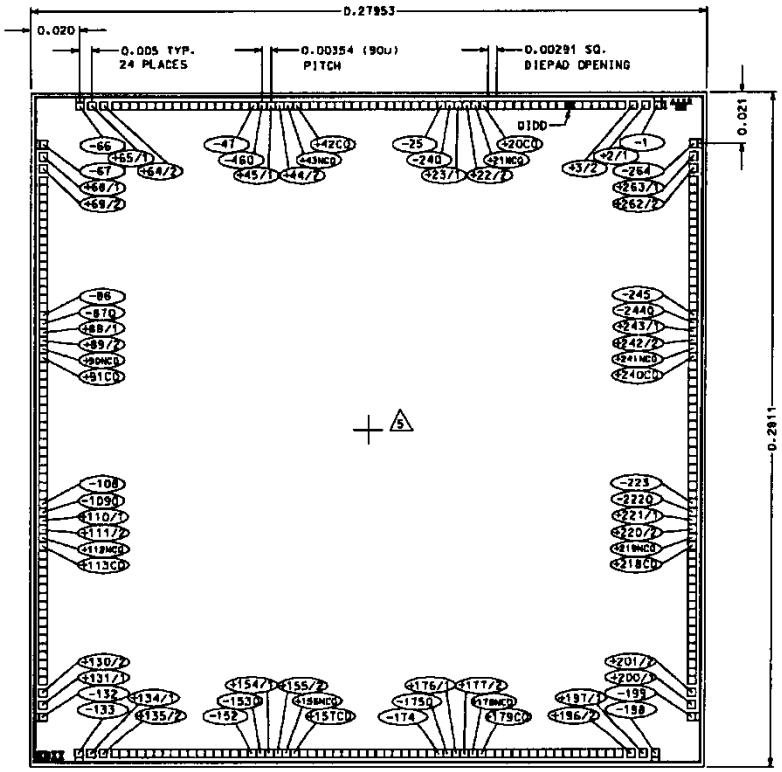
60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

DIEPAD XY LOCATION TABLE (MILS)

DIEPAD	X	Y	DIEPAD	X	Y	DIEPAD	X	Y	DIEPAD	X	Y
1	119.6	135.3	67	-134.7	119.5	133	-119.6	-135.4	199	134.6	-119.6
2	114.6	135.3	68	-134.7	114.5	134	-114.6	-135.4	200	134.6	-114.6
3	109.6	135.3	69	-134.7	109.5	135	-109.6	-135.4	201	134.6	-109.6
4	104.6	135.3	70	-134.7	104.5	136	-104.6	-135.4	202	134.6	-104.6
5	101.0	135.3	71	-134.7	101.0	137	-101.0	-135.4	203	134.6	-101.1
6	97.5	135.3	72	-134.7	97.4	138	-97.5	-135.4	204	134.6	-97.5
7	93.9	135.3	73	-134.7	93.9	139	-93.9	-135.4	205	134.6	-94.0
8	90.4	135.3	74	-134.7	90.3	140	-90.4	-135.4	206	134.6	-90.5
9	86.9	135.3	75	-134.7	86.8	141	-86.9	-135.4	207	134.6	-86.9
10	83.3	135.3	76	-134.7	83.3	142	-83.3	-135.4	208	134.6	-83.4
11	79.8	135.3	77	-134.7	79.7	143	-79.8	-135.4	209	134.6	-79.8
12	76.2	135.3	78	-134.7	76.2	144	-76.2	-135.4	210	134.6	-76.3
13	72.7	135.3	79	-134.7	72.6	145	-72.7	-135.4	211	134.6	-72.7
14	69.1	135.3	80	-134.7	69.1	146	-69.1	-135.4	212	134.6	-69.2
15	65.6	135.3	81	-134.7	65.5	147	-65.6	-135.4	213	134.6	-65.7
16	62.1	135.3	82	-134.7	62.0	148	-62.1	-135.4	214	134.6	-62.1
17	58.5	135.3	83	-134.7	58.5	149	-58.5	-135.4	215	134.6	-58.6
18	55.0	135.3	84	-134.7	54.9	150	-55.0	-135.4	216	134.6	-55.0
19	51.4	135.3	85	-134.7	51.4	151	-51.4	-135.4	217	134.6	-51.5
20	47.9	135.3	86	-134.7	47.8	152	-47.9	-135.4	218	134.6	-47.9
21	44.3	135.3	87	-134.7	44.3	153	-44.3	-135.4	219	134.6	-44.4
22	40.8	135.3	88	-134.7	40.7	154	-40.8	-135.4	220	134.6	-40.8
23	37.3	135.3	89	-134.7	37.2	155	-37.2	-135.4	221	134.6	-37.3
24	33.7	135.3	90	-134.7	33.7	156	-33.7	-135.4	222	134.6	-33.8
25	30.2	135.3	91	-134.7	30.1	157	-30.2	-135.4	223	134.6	-30.2
26	26.6	135.3	92	-134.7	26.6	158	-26.6	-135.4	224	134.6	-26.7
27	23.1	135.3	93	-134.7	23.0	159	-23.1	-135.4	225	134.6	-23.1
28	19.5	135.3	94	-134.7	19.5	160	-19.5	-135.4	226	134.6	-19.6
29	16.0	135.3	95	-134.7	15.9	161	-16.0	-135.4	227	134.6	-16.0
30	12.5	135.3	96	-134.7	12.4	162	-12.4	-135.4	228	134.6	-12.5
31	8.9	135.3	97	-134.7	8.8	163	-8.9	-135.4	229	134.6	-9.0
32	5.4	135.3	98	-134.7	5.3	164	-5.4	-135.4	230	134.6	-5.4
33	1.8	135.3	99	-134.7	1.8	165	-1.8	-135.4	231	134.6	-1.9
34	-1.8	135.3	100	-134.7	-1.9	166	1.8	-135.4	232	134.6	1.8
35	-5.4	135.3	101	-134.7	-5.4	167	5.4	-135.4	233	134.6	5.3
36	-8.9	135.3	102	-134.7	-9.0	168	8.9	-135.4	234	134.6	8.8
37	-12.4	135.3	103	-134.7	-12.5	169	12.5	-135.4	235	134.6	12.4
38	-16.0	135.3	104	-134.7	-16.0	170	16.0	-135.4	236	134.6	15.9
39	-19.5	135.3	105	-134.7	-19.6	171	19.5	-135.4	237	134.6	19.5
40	-23.1	135.3	106	-134.7	-23.1	172	23.1	-135.4	238	134.6	23.0
41	-26.6	135.3	107	-134.7	-26.7	173	26.6	-135.4	239	134.6	26.6
42	-30.2	135.3	108	-134.7	-30.2	174	30.2	-135.4	240	134.6	30.1
43	-33.7	135.3	109	-134.7	-33.8	175	33.7	-135.4	241	134.6	33.7
44	-37.2	135.3	110	-134.7	-37.3	176	37.3	-135.4	242	134.6	37.2
45	-40.8	135.3	111	-134.7	-40.8	177	40.8	-135.4	243	134.6	40.7
46	-44.3	135.3	112	-134.7	-44.4	178	44.3	-135.4	244	134.6	44.3
47	-47.9	135.3	113	-134.7	-47.9	179	47.9	-135.4	245	134.6	47.8
48	-51.4	135.3	114	-134.7	-51.5	180	51.4	-135.4	246	134.6	51.4
49	-55.0	135.3	115	-134.7	-55.0	181	55.0	-135.4	247	134.6	54.9
50	-58.5	135.3	116	-134.7	-58.6	182	58.5	-135.4	248	134.6	58.5
51	-62.1	135.3	117	-134.7	-62.1	183	62.1	-135.4	249	134.6	62.0
52	-65.6	135.3	118	-134.7	-65.7	184	65.6	-135.4	250	134.6	65.5
53	-69.1	135.3	119	-134.7	-69.2	185	69.1	-135.4	251	134.6	69.1
54	-72.7	135.3	120	-134.7	-72.7	186	72.7	-135.4	252	134.6	72.6
55	-76.2	135.3	121	-134.7	-76.3	187	76.2	-135.4	253	134.6	76.2
56	-79.8	135.3	122	-134.7	-79.8	188	79.8	-135.4	254	134.6	79.7
57	-83.3	135.3	123	-134.7	-83.4	189	83.3	-135.4	255	134.6	83.3
58	-86.9	135.3	124	-134.7	-86.9	190	86.9	-135.4	256	134.6	86.8
59	-90.4	135.3	125	-134.7	-90.5	191	90.4	-135.4	257	134.6	90.3
60	-93.9	135.3	126	-134.7	-94.0	192	93.9	-135.4	258	134.6	93.9
61	-97.5	135.3	127	-134.7	-97.5	193	97.5	-135.4	259	134.6	97.4
62	-101.0	135.3	128	-134.7	-101.1	194	101.0	-135.4	260	134.6	101.0
63	-104.6	135.3	129	-134.7	-104.6	195	104.6	-135.4	261	134.6	104.5
64	-109.6	135.3	130	-134.7	-109.6	196	109.6	-135.4	262	134.6	109.5
65	-114.6	135.3	131	-134.7	-114.6	197	114.6	-135.4	263	134.6	114.5
66	-119.6	135.3	132	-134.7	-119.6	198	119.6	-135.4	264	134.6	119.5

FIGURE A-1. Die bonding pad locations and electrical functions.



Notes:
1. All dimensions are in inches and are basic.
2. Backside bias is V_{SS}.
3. Die backside is as lapped.
4. Die center is the coordinate origin (0,0).
5. Diepad 10 is reserved for use with QIDD test.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 0.29753 x 0.2811
Die thickness: 0.0175 ± 0.001

Interface materials.
Top metallization: Si Al Cu 6.2 kA – 7.6 kA
Backside metallization: None

Glassivation.
Type: Oxide/Nitride
Thickness: 9 kA – 11 kA

Substrate: Epitaxial layer on Single crystal silicon

Assembly related information.
Substrate potential: Tied to V_{SS}
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

ID	X	Y	ID	X	Y	ID	X	Y
1	165.0	185.9	37	-61.8	185.9	73	-184.6	56.7
2	158.7	185.9	38	-68.1	185.9	74	-184.6	50.4
3	152.4	185.9	39	-74.4	185.9	75	-184.6	44.1
4	146.1	185.9	40	-80.7	185.9	76	-184.6	37.8
5	139.8	185.9	41	-87.0	185.9	77	-184.6	31.5
6	133.5	185.9	42	-93.3	185.9	78	-184.6	25.2
7	127.2	185.9	43	-99.6	185.9	79	-184.6	18.9
8	120.9	185.9	44	-105.9	185.9	80	-184.6	12.6
9	114.6	185.9	45	-112.2	185.9	81	-184.6	6.3
10	108.3	185.9	46	-118.5	185.9	82	-184.6	0.0
11	102.0	185.9	47	-124.8	185.9	83	-184.6	-6.3
12	95.7	185.9	48	-131.1	185.9	84	-184.6	-12.6
13	89.4	185.9	49	-137.4	185.9	85	-184.6	-18.9
14	83.1	185.9	50	-143.7	185.9	86	-184.6	-25.2
15	76.8	185.9	51	-150.0	185.9	87	-184.6	-31.5
16	70.5	185.9	52	-156.3	185.9	88	-184.6	-37.8
17	64.2	185.9	53	-162.6	185.9	89	-184.6	-44.1
18	57.9	185.9	54	-168.9	185.9	90	-184.6	-50.4
19	51.6	185.9	55	-184.6	170.2	91	-184.6	-56.7
20	45.3	185.9	56	-184.6	163.9	92	-184.6	-63.0
21	39.0	185.9	57	-184.6	157.4	93	-184.6	-69.3
22	32.7	185.9	58	-184.6	151.1	94	-184.6	-75.6
23	26.4	185.9	59	-184.6	144.8	95	-184.6	-81.9
24	20.1	185.9	60	-184.6	138.5	96	-184.6	-88.2
25	13.8	185.9	61	-184.6	132.2	97	-184.6	-94.5
26	7.5	185.9	62	-184.6	125.9	98	-184.6	-100.8
27	1.2	185.9	63	-184.6	119.6	99	-184.6	-107.1
28	-5.1	185.9	64	-184.6	113.3	100	-184.6	-113.4
29	-11.4	185.9	65	-184.6	107.1	101	-184.6	-119.7
30	-17.7	185.9	66	-184.6	100.8	102	-184.6	-126.0
31	-24.0	185.9	67	-184.6	94.5	103	-184.6	-132.3
32	-30.3	185.9	68	-184.6	88.2	104	-184.6	-138.6
33	-36.6	185.9	69	-184.6	81.9	105	-184.6	-144.9
34	-42.9	185.9	70	-184.6	75.6	106	-184.6	-151.2
35	-49.2	185.9	71	-184.6	69.3	107	-184.6	-157.5
36	-55.5	185.9	72	-184.6	63.0	108	-184.6	-164.0

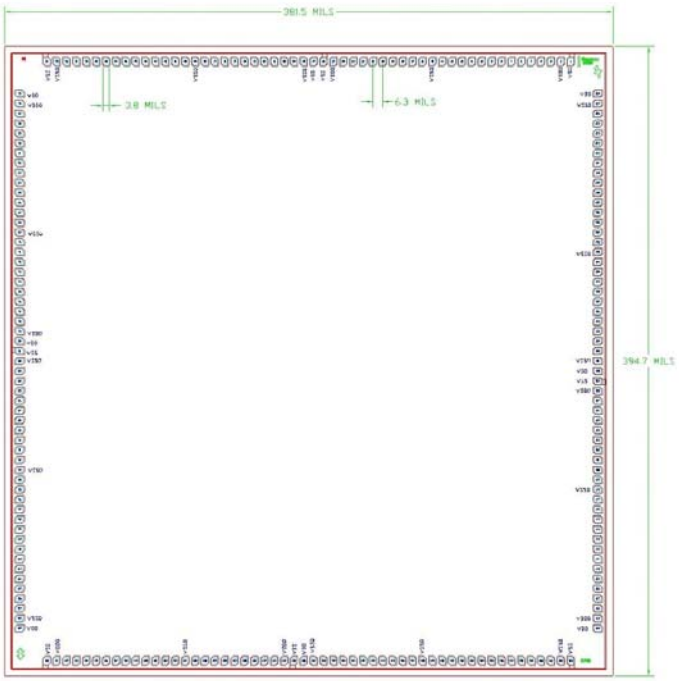
Note: Die dimensions are in mils and X, Y distances are from center of the die

FIGURE A-2 Die bonding pad locations

ID	X	Y	ID	X	Y	ID	X	Y
109	-184.6	-170.3	146	57.9	-186.0	183	180.7	-50.4
110	-168.9	-186.0	147	64.2	-186.0	184	180.7	-44.1
111	-162.6	-186.0	148	70.5	-186.0	185	180.7	-37.8
112	-156.3	-186.0	149	76.8	-186.0	186	180.7	-31.5
113	-150.0	-186.0	150	83.1	-186.0	187	180.7	-25.2
114	-143.7	-186.0	151	89.4	-186.0	188	180.7	-18.9
115	-137.4	-186.0	152	95.7	-186.0	189	180.7	-12.6
116	-131.1	-186.0	153	102.0	-186.0	190	180.7	-6.3
117	-124.8	-186.0	154	108.3	-186.0	191	180.7	0.0
118	-118.5	-186.0	155	114.6	-186.0	192	180.7	6.3
119	-112.2	-186.0	156	120.9	-186.0	193	180.7	12.6
120	-105.9	-186.0	157	127.2	-186.0	194	180.7	18.9
121	-99.6	-186.0	158	133.5	-186.0	195	180.7	25.2
122	-93.3	-186.0	159	139.8	-186.0	196	180.7	31.5
123	-87.0	-186.0	160	146.1	-186.0	197	180.7	37.8
124	-80.7	-186.0	161	152.4	-186.0	198	180.7	44.1
125	-74.4	-186.0	162	158.7	-186.0	199	180.7	50.4
126	-68.1	-186.0	163	165.0	-186.0	200	180.7	56.7
127	-61.8	-186.0	164	180.7	-170.3	201	180.7	63.0
128	-55.5	-186.0	165	180.7	-163.8	202	180.7	69.3
129	-49.2	-186.0	166	180.7	-157.5	203	180.7	75.6
130	-42.9	-186.0	167	180.7	-151.2	204	180.7	81.9
131	-36.6	-186.0	168	180.7	-144.9	205	180.7	88.2
132	-30.3	-186.0	169	180.7	-138.6	206	180.7	94.5
133	-24.0	-186.0	170	180.7	-132.3	207	180.7	100.8
134	-17.7	-186.0	171	180.7	-126.0	208	180.7	107.1
135	-11.4	-186.0	172	180.7	-119.7	209	180.7	113.4
136	-5.1	-186.0	173	180.7	-113.4	210	180.7	119.7
137	1.2	-186.0	174	180.7	-107.1	211	180.7	126.0
138	7.5	-186.0	175	180.7	-100.8	212	180.7	132.3
139	13.8	-186.0	176	180.7	-94.5	213	180.7	138.6
140	20.1	-186.0	177	180.7	-88.2	214	180.7	144.9
141	26.4	-186.0	178	180.7	-81.9	215	180.7	151.2
142	32.7	-186.0	179	180.7	-75.6	216	180.7	157.6
143	39.0	-186.0	180	180.7	-69.3	217	180.7	163.9
144	45.3	-186.0	181	180.7	-63.0	218	180.7	170.2
145	51.6	-186.0	182	180.7	-56.7			

Note: Die dimensions are in mils and X, Y distances are from center of the die

FIGURE A-2 Die bonding pad locations - Continued



NOTES:

1. All dimensions are in inches and are basic.
2. Backside bias is V_{SS}.
3. Die backside is as lapped.
4. Die center is the coordinate origin (0,0).

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 0.3851 x 0.3947
Die thickness: 0.0175 ± 0.001

Interface materials.
Top metallization: Si -Cu 6.8 kA
Backside metallization: None

Glassivation.
Type: Oxide/Nitride
Thickness: 5 kA – 12 kA

Substrate: Epitaxial layer on Single crystal silicon

Assembly related information.
Substrate potential: Tied to V_{SS}
Special assembly instructions: None

FIGURE A-2. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-11-23

Approved sources of supply for SMD 5962-99B01 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/ 2/	Vendor CAGE number	Vendor similar PIN 3/
5962F99B0101Q_C 5962F99B0101V_C	65342	UT06MRA010
5962R99B0101Q9A 5962R99B0101V9A	65342	UT06MRA010_QDIE UT06MRA010_VDIE
5962F99B0102Q_C 5962F99B0102V_C	65342	UT06MRA025
5962R99B0102Q9A 5962R99B0102V9A	65342	UT06MRA025_QDIE UT06MRA025_VDIE
5962F99B0103Q_C 5962F99B0103V_C	65342	UT06MRA050
5962F99B0104Q_C 5962F99B0104V_C	65342	UT06MRA075
5962R99B0105Q_C 5962R99B0105V_C	65342	UT06MRA100
5962R99B0106Q_C 5962R99B0106V_C	65342	UT06MRA150
5962R99B0107Q_C 5962R99B0107V_C	65342	UT06MRA200
5962R99B0108Q_C 5962R99B0108V_C	65342	UT06MRA250
5962R99B0109Q_C 5962R99B0109V_C	65342	UT06MRA300
5962R99B0110Q_C 5962R99B0110V_C	65342	UT06MRA350
5962R99B0111Q_C 5962R99B0111V_C	65342	UT06MRA400
5962R99B0112Q_C 5962R99B0112V_C	65342	UT06MRA450
5962R99B0113Q_C 5962R99B0113V_C	65342	UT06MRA500
5962-99B0114Q_C 5962R99B0114V_C	4/	UT06MRA550
5962-99B0115Q_C 5962R99B0115V_C	4/	UT06MRA600

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Due to the nature of this SMD, the standard microcircuit drawing PIN and corresponding vendor similar PIN shall be specified in the AID. The vendor similar PIN will be based on the UT06MRA gate array family. Contact the listed approved source of supply for availability of case outlines (defined in 1.2.4) for each device.

3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

4/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Blvd. Colorado Springs, CO 80907-3486