

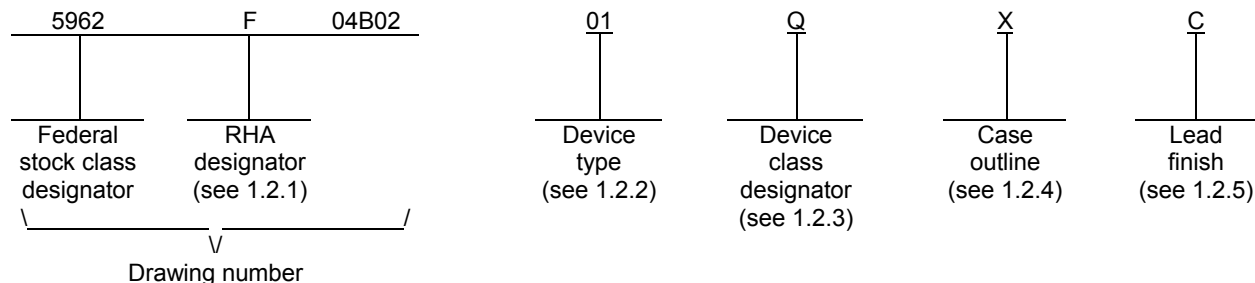
REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add total dose rate for design dependent in 1.5 Radiation features. - phn	05-11-01	Thomas M. Hess
B	Change footnote 7/ on table I. Correct the wording "Accelerated annealing testing" in section 4.4.4.1.1 for RHA device testing. - phn	07-02-26	Thomas M. Hess
C	Change maximum voltage difference in 1.3. Correct footnote 3/ and 8/ in table I. - phn	07-06-20	Thomas M. Hess
D	Correct test conditions for V _{OH} and V _{OL} in table I. - phn	08-01-16	Thomas M. Hess

REV																				
SHEET																				
REV				B																
SHEET	15	16	17	18	19															
REV STATUS				REV		D	C				D	B	C							
OF SHEETS				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14	
PMIC N/A				PREPARED BY Phu H. Nguyen					DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dscc.dla.mil											
STANDARD MICROCIRCUIT DRAWING				CHECKED BY Phu H. Nguyen																
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE				APPROVED BY Thomas M. Hess					MICROCIRCUIT, DIGITAL, 0.25 μm STANDARD CELL, GATE ARRAY, RADIATION HARDENED, MONOLITHIC SILICON											
				DRAWING APPROVAL DATE 05-06-15																
				REVISION LEVEL D																
AMSC N/A									SHEET		1 OF 19									

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Signal I/O 2/	Power & Ground Pads 3/
01	25RHD05	Up to 500,000 gates	310	72
02	25RHD20	Up to 2,000,000 gates	384	136
03	25RHD30	Over 2,000,000 gates	460	198

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	208	Ceramic flatpack
Y	See figure 1	256	Ceramic flatpack
Z	See figure 1	352	Ceramic flatpack
U	See figure 1	472	Land grid array

1/ These devices are capable of being configured and support dual voltage: 2.5 V core / 3.3 V I/O bus.
 2/ Includes 5 pins that may or may not be reserved for JTAG boundary scan.
 3/ Reserved for dedicated V_{DD}/V_{SS} and V_{DDQ}/V_{SSQ}.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 2

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 4/

I/O DC Supply Voltage (V_{DD})	-0.3 V to 4.0 V
Core DC Supply Voltage (V_{DDCORE})	-0.3 V to 2.8 V
Maximum Voltage on any pin (V_{IO})	
CMOS, Schmitt.....	-0.3 V to $V_{DD}+0.3$ V
Cold-spares	-0.3 V to $V_{DD}+0.3$ V
PCI	-0.5 V to $V_{DD}+0.5$ V
Inputs.....	3.6 V
Inputs (5.0 V Tolerant)	5.5 V
Maximum Voltage Difference ($V_{DD} - V_{DDCORE}$).....	1.35 V
Storage temperature (T_{STG})	-65°C to +150°C
Maximum junction temperature (T_J).....	+150°C 5/
Latch up immunity (I_{LU})	±150 mA
DC input current (I_i)	±10 mA
Lead Temperature (soldering 5 sec).....	+300°C

1.3.1 I/O Signal undershoot/overshoot. 6/

Maximum overshoot on any I/O pad	
10 MHz	$V_{DD}+2.5$ V
33 MHz	$V_{DD}+1.6$ V
50 MHz	$V_{DD}+1.3$ V
100 MHz	$V_{DD}+1.0$ V
Minimum undershoot on any I/O pad	
10 MHz	-2.5 V
33 MHz	-1.6 V
50 MHz	-1.3 V
100 MHz	-1.0 V

1.4 Recommended operating conditions.

I/O DC Supply Voltage (V_{DD})	3.0 V to 3.6 V
Core DC Supply Voltage (V_{DDCORE}).....	2.25 V to 2.75 V
Case temperature range (T_C).....	-55°C to +125°C
DC input voltage (V_{IN})	0 V to V_{DD} 7/

1.5 Radiation features.

Total dose (Dose rate = 50 – 300 Rad(Si)/s)	≥ 1 x 10 ⁵ Rads (Si) 8/
Total dose (Dose rate = 50 – 300 Rad(Si)/s)	≥ 3 x 10 ⁵ Rads (Si) 9/
Single event phenomenon (SEP) effective	
LET, no upset	10/
LET, no latchup	≥ 100 MeV-cm ² /mg

1.6 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) as specified in the AID

- 4/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 5/ Design flow includes a worst case electromigration analysis during place and route, including derating for maximum junction temperature and customer specified maximum operating frequency (MHz) and device operating life time (years). Additional power dissipation and package thermal analysis is provided to the customer to advise them of the maximum package case temperature T_C allowed to maintain the junction temperature T_J within the recommended operating temperature range.
- 6/ Assuming a maximum under/overshoot pulse width of 3 ns.
- 7/ Input buffers are 5 V tolerant.
- 8/ The dose rate shall be 50 – 300 Rad(Si)/s unless otherwise specified in the AID.
- 9/ Design dependent. The dose rate shall be 50 – 300 Rad(Si)/s unless otherwise specified in the AID.
- 10/ When characterized as a result of the procuring activities request, the condition will be specified.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL C	SHEET 3

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

- MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.
- MIL-PRF-55681 - Capacitor, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

- MIL-STD-883 - Test Method Standard Microcircuits.
- MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

- MIL-HDBK-103 - List of Standard Microcircuit Drawings.
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non Government publications. The following document(s) for a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 – IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer’s Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and as specified in figure 1.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 4

3.3 AID requirements. All AIDs written against this SMD shall be sent to DSCC-VA. The following items shall be provided to the device manufacturer by the customer as part of an AID.

3.3.1 Terminal connections and pin assignments.

3.3.2 Package type (see 1.2.4).

3.3.3 Functional block diagram (or equivalent HDL behavioral description).

3.3.4 Functional description terms and symbols.

3.3.5 Logic diagram (or equivalent structural HDL description or mutually agreed to net list).

3.3.6 Pin function description.

3.3.7 Design tape # or Design document name (i.e., net list).

3.3.8 Design functional tape # or name.

3.3.9 Test functional tape # or name.

3.3.10 Timing diagram(s).

3.3.11 Fault coverage measurement of manufacturing logic tests.

3.3.12 Burn-in circuit.

3.3.13 ESD class and voltage.

3.3.14 Device electrical performance characteristics (additions to Table I). Device electrical performance characteristics shall include dc parametric, functional, ac parameters and any other data which would be considered required by a design engineer. All electrical performance characteristics apply over the full recommended ambient operating temperature range and specified test load conditions.

3.3.15 Maximum power dissipation. Maximum power dissipation shall be in accordance with the application specific design.

3.3.16 Supply voltage range. The supply voltage range shall be as specified in the AID.

3.3.17 Dose rate. The dose rate shall be 50 – 300 Rad(Si)/s unless otherwise specified in the AID.

3.4 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.6.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 5

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.10 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 6

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _C ≤ +125°C V _{DD} = 3.3 V ± 0.3 V V _{DDC} = 2.5 V ± 0.25 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low-level input voltage CMOS inputs <u>3/</u> PCI inputs <u>3/</u> LVTTTL	V _{IL}	V _{DD} = 3.0 V and 3.6 V	1, 2, 3	All		0.3V _{DD} 0.3V _{DD} 0.8	V
High-level input voltage CMOS inputs <u>3/</u> PCI inputs <u>3/</u> LVTTTL	V _{IH}	V _{DD} = 3.0 V and 3.6 V	1, 2, 3	All	0.7V _{DD} 0.5V _{DD} 2.0		V
Schmitt Trigger, positive going threshold <u>3/</u>	V _{T+}	V _{DD} = 3.0 V and 3.6 V	1, 2, 3	All		0.7V _{DD}	V
Schmitt Trigger, negative going threshold <u>3/</u>	V _{T-}	V _{DD} = 3.0 V and 3.6 V	1, 2, 3	All	0.3V _{DD}		V
Schmitt Trigger, typical range of hysteresis <u>4/</u>	V _H		1, 2, 3	All	0.4		V
Input leakage current Inputs with pull-down resistors Inputs with pull-down resistors Inputs with pull-up resistors Inputs with pull-up resistors Cold spare inputs – “Off” Cold spare inputs – “On”	I _{IN}	V _{DD} = Operating mode V _{IN} = V _{DD} V _{IN} = V _{SS} V _{IN} = V _{DD} V _{IN} = V _{SS} V _{IN} = V _{DD} or V _{SS} V _{DDC} = V _{DD} = V _{SS} = 0 V V _{IN} = 0 V or 3.6 V V _{IN} = 5.5 V	1, 2, 3	All	10 -5 -5 -120 -5 -5 -10 -10	120 5 5 -10 5 5 10	μA
Low-level output voltage LVTTTL buffer LVTTTL buffer LVTTTL buffer LVTTTL buffer LVTTTL buffer CMOS outputs CMOS outputs PCI outputs	V _{OL}	V _{DD} = 3.0 V I _{OL} = 4.0 mA I _{OL} = 5.0 mA I _{OL} = 8.0 mA I _{OL} = 12.0 mA I _{OL} = 24.0 mA I _{OL} = 1.0 μA I _{OL} = 100.0 μA I _{OL} = 1500.0 μA	1, 2, 3	All		0.4 0.4 0.4 0.4 0.4 0.05 0.25 0.1V _{DD}	V
High-level output voltage LVTTTL buffer LVTTTL buffer LVTTTL buffer LVTTTL buffer LVTTTL buffer CMOS outputs CMOS outputs PCI outputs	V _{OH}	V _{DD} = 3.0 V I _{OH} = -4.0 mA I _{OH} = -5.0 mA I _{OH} = -8.0 mA I _{OH} = -12.0 mA I _{OH} = -24.0 mA I _{OH} = -1.0 μA I _{OH} = -100.0 μA I _{OH} = -500.0 μA	1, 2, 3	All	2.4 2.4 2.4 2.4 2.4 V _{DD} - 0.05 V _{DD} - 0.35 0.9V _{DD}		V

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL D	SHEET 7

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _C ≤ +125°C V _{DD} = 3.3 V ± 0.3 V V _{DCC} = 2.5 V ± 0.25 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Three-state output leakage current Bidirect with pull-up resistor Bidirect with pull-up resistor Bidirect with pull-down resistor Bidirect with pull-down resistor Cold spare bidirect – “On” Cold spare bidirect – “Off”	I _{OZ}	V _{DD} = Operating mode V _O = V _{DD} V _O = V _{SS} V _O = V _{DD} V _O = V _{SS} V _{IN} = 0 V or 3.6 V V _{DCC} = V _{DD} = V _{SS} = 0 V V _{IN} = V _{DD} or V _{SS}	1, 2, 3	All	-10 -120 20 -10 -10	10 -10 150 10 10	μA
Short-circuit output current <u>4/ 6/</u> CMOS, 4 mA buffer CMOS, 8 mA buffer CMOS, 12 mA buffer PCI	I _{OS}	V _O = V _{DD} = V _{SS} V _O = V _{DD} = V _{SS} V _O = V _{DD} = V _{SS} V _O = V _{DD} = V _{SS}	1, 2, 3	All	-40 -50 -65 -130	70 100 130 270	mA
Quiescent supply current <u>7/</u>	I _{DDQ}	V _{DD} = 3.6 V V _{DD} = 3.6 V V _{DD} = 3.6 V M, D, P, L, R, F	1,3 2 1	All All All	 8	<u>7/</u> 8	μA mA mA
Input capacitance <u>8/</u> CMOS and LVTTTL output capacitance <u>8/</u> 3.0 mA buffers 5.0 mA buffers 9.0 mA buffers 12.0 mA buffers	C _{IN} C _{OUT}	f = 1 MHz at 0 V f = 1 MHz at 0 V	4 4	All All	4	12 10 12 20 25	pF
CMOS output capacitance <u>8/</u> 3.0 mA buffers 5.0 mA buffers 9.0 mA buffers 12.0 mA buffers	C _{I/O}	f = 1 MHz at 0 V	4	All		15 18 20 25	
LVDS input capacitance <u>8/</u>	C _{IN}	f = 1 MHz at 0 V	4	All		16	
LVDS output capacitance <u>8/</u>	C _{OUT}	f = 1 MHz at 0 V	4	All		19	
PCI bidirect capacitance <u>8/</u>	C _{I/O}	f = 1 MHz at 0 V	4	All		13	
Cold spare leakage current LVDS	I _{CS}	V _{IN} = 3.6 V, V _{DD} = V _{SS} = 0	1, 2, 3	All	-10	10	μA
Differential output voltage LVDS	V _{OD1}	R _L = 100 Ω	1, 2, 3	All	250	800	mV
Offset voltage LVDS	V _{OS}	R _L = 100 Ω	1, 2, 3	All	1.12	1.6	V
Change in magnitude of V _{OD1} for complementary output states LVDS	Δ V _{OD1}	R _L = 100 Ω	1, 2, 3	All		35	mV
Change in magnitude of V _{OS} for complementary output states LVDS	Δ V _{OS}	R _L = 100 Ω	1, 2, 3	All		25	
Output short circuit current LVDS <u>4/ 6/</u>	I _{OS}	V _{IN} = V _{DD} , V _{OUT+} = 0 V or V _{IN} = GND, V _{OUT-} = 0 V	1, 2, 3	All		9.0	mA
Output tri state current LVDS	I _{OZ}	Output disabled, V _{DD} = 3.6 V V _{OUT} = 0 V or V _{DD} ,	1, 2, 3	All			μA

See notes at end of table

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL B	SHEET 8

TABLE I. Electrical performance characteristics – Continued..

Notes:

- 1/ Devices supplied to this drawing will meet all levels M, D, P, L, R and F of irradiation. However, this device is only tested at the 'F' level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, $T_A = +25\text{ C}$.
- 2/ Proper power up and power down sequencing is required to avoid establishing an IOS (Output short circuit) condition between UT0.25 μ HBD device I/O buffers and the signals of external devices.
 - V_{SSQ} (core ground) and V_{SS} (I/O ground) connections must be tied to a common ground reference (i.e., power supply ground or chassis).
 - During power up sequencing, V_{DDQ} shall be applied before V_{DD} .
 - During power up, a reset signal should be applied before or concurrent with V_{DD} exceeding 200 mV and maintained for at least 1 ms after V_{DD} exceeds 3.0 V.
 - During power down, V_{DD} shall be removed before V_{DDQ} .
 - During the power up/ power down sequence when V_{DD} is not applied, V_{DD} should be disconnected from the ground (i.e. floating or impedance to ground $> 10\ \Omega$) because V_{DDQ} pulls V_{DD} up through a diode drop due to built in ESD protection circuitry.
 - Cold spare mode: whenever the V_{DD} and V_{DDQ} supplies are both below 200 mV, the device will be cold spared (i.e. Input/Output buffers are in high impedance state)

The UT0.25 μ HBD technology is robust and can tolerance power up/ down sequences which are not fully compliant with these requirements. Please contact the factory to review sequences that do not comply with that prescribed above.
- 3/ Functional tests are conducted in accordance with MIL-STD-883 with the following input conditions:
 $V_{IH} = V_{IH(min)} + 20\%$, $- 0\%$; $V_{IL} = V_{IL(max)} + 0\%$, -50% , as specified herein for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.
- 4/ Supplied as a design limit but not guaranteed or tested.
- 5/ Device inputs are 5.0 V tolerant and have been verified to meet leakage specifications.
- 6/ Not more than one output may be shorted at a time for maximum duration of one second.
- 7/ Quiescent currents are relative to the core supply, V_{DDCore} . All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low. I_{DDQ} will be set to 35 μ A for room temperature package level testing unless otherwise specified in AID.
- 8/ Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1 MHz @ 0 V and a signal amplitude of ≤ 50 mV RMS. Capacitance numbers include package capacitance without external chip capacitors attached.

TABLE IB. SEP test limits. 1/ 2/

Device Type	$T_A = \text{Temperature } \pm 10^\circ\text{C}$	SEU BIAS, $V_{DD} = 3.0\text{ V}$ I/O, 2.25 V core		Bias for latch-up test $V_{DD} = 3.6\text{ V}$ I/O, 2.75 V core no latch-up LET
		Effective LET no upsets [MEV – cm^2/mg]	Maximum device cross section (μm^2) (LET = 100)	
All	3/	4/	4/	4/

NOTE: Devices that contain cross coupled resistance must be tested at the maximum rated T_A .

- 1/ For SEP test conditions, see 4.4.4.5 herein.
- 2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
- 3/ Worst case temperature for latch up testing $T_A = +125^\circ\text{C}$; worst case temperature for upset testing $T_A = +25^\circ\text{C}$;
- 4/ When characterized as a result of the procuring activities request, this parameter will be specified.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL C	SHEET 9

Case X

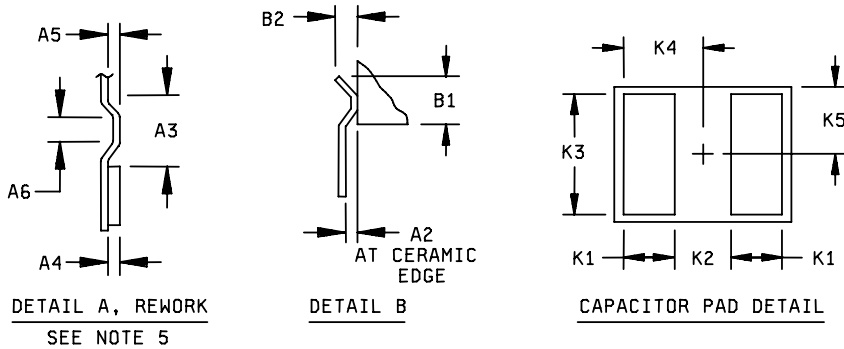
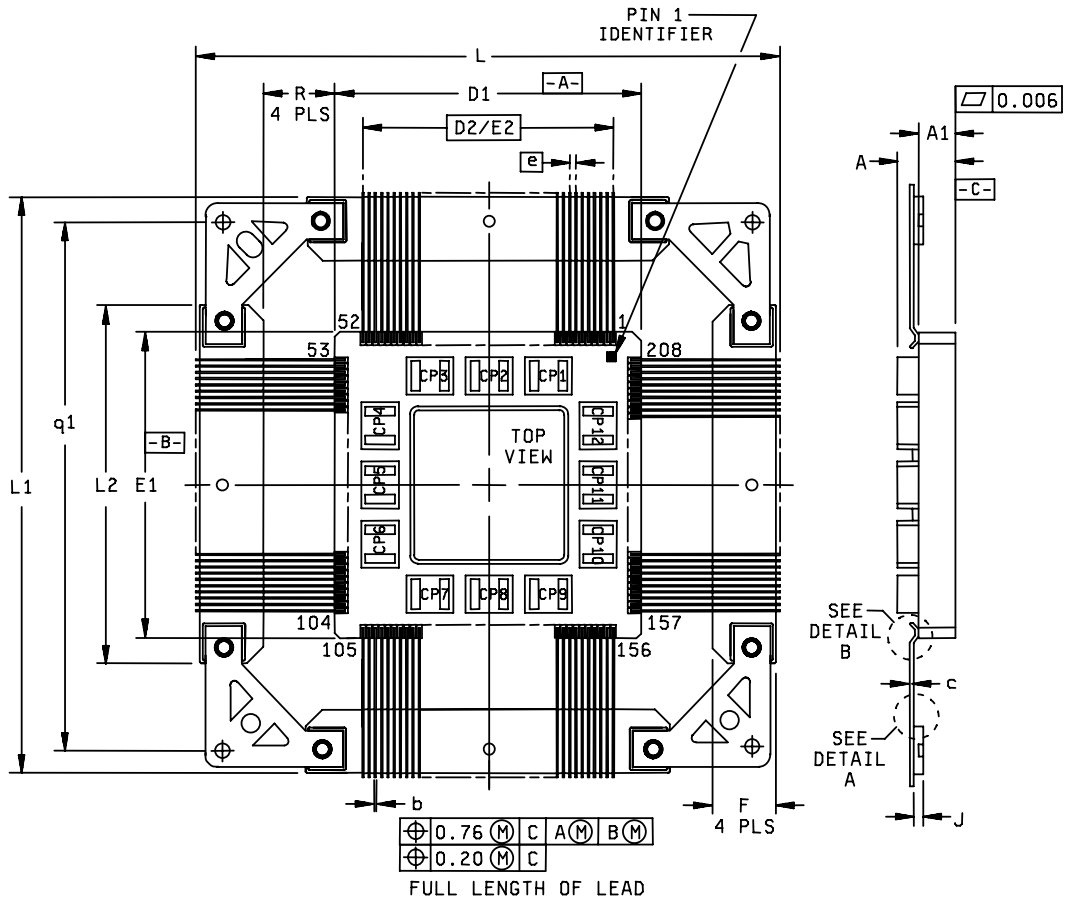


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 10

Case X - Continued

CP1	V _{DD1}	CP5	V _{DDCQ}	CP9	V _{DD1}
CP2	V _{DDCQ}	CP6	V _{DD1}	CP10	V _{DD1}
CP3	V _{DD1}	CP7	V _{DD1}	CP11	V _{DDCQ}
CP4	V _{DD1}	CP8	V _{DD1}	CP12	V _{DD1}

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.167		.164
A1	2.06	2.50	.081	.099
A2		0.25		.010
A3		1.90		.075
A4	0.89 REF		.035 REF	
A5		0.89		.035
A6	1.27 REF		.050 REF	
B1		0.71		.028
B2		0.36		.014
b	0.15	0.25	.005	.010
c	0.10	0.20	.004	.008
e	0.50 BSC		.0197 BSC	
F		7.75		.306
D1/e1	27.86	28.12	1.097	1.107
D2/E2	25.50 BSC		1.004 BSC	
L		77.22		3.040
L1		75.00		2.953
L2	55.79	56.81	2.196	2.237
K1	1.40		.055	
K2	1.65		.065	
K3	2.79		.110	
K4	2.22		.087	
K5	1.40		.055	
q1		70.00		2.756
R	14.50		.570	
J	0.77	1.03	.030	.041

Notes:

1. All exposes metalized areas are gold plated over nickel plating.
2. The lid is connected to V_{SS}.
3. Capacitors pads are designed for a MIL-PRF-55681 CDR33BX, 50V .1μF chip cap.
4. Tiebar areas may have notches and tabs different than shown.
5. Packages may be shipped with repaired leads as shown. Coplanarity requirements do not apply in repaired areas.

FIGURE 1. Case outline - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 11

Case Y

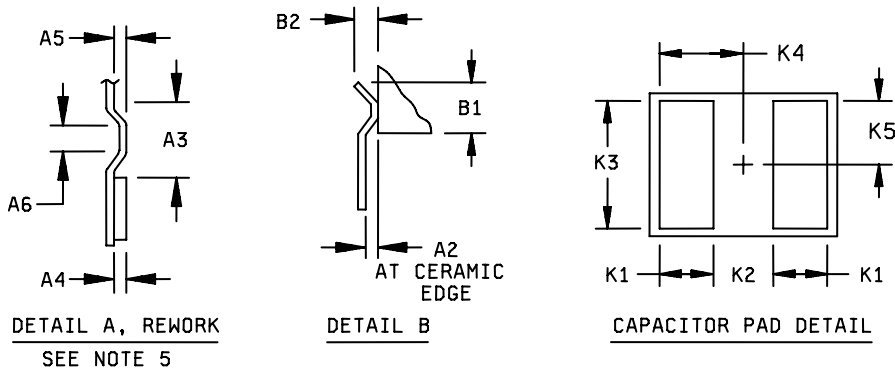
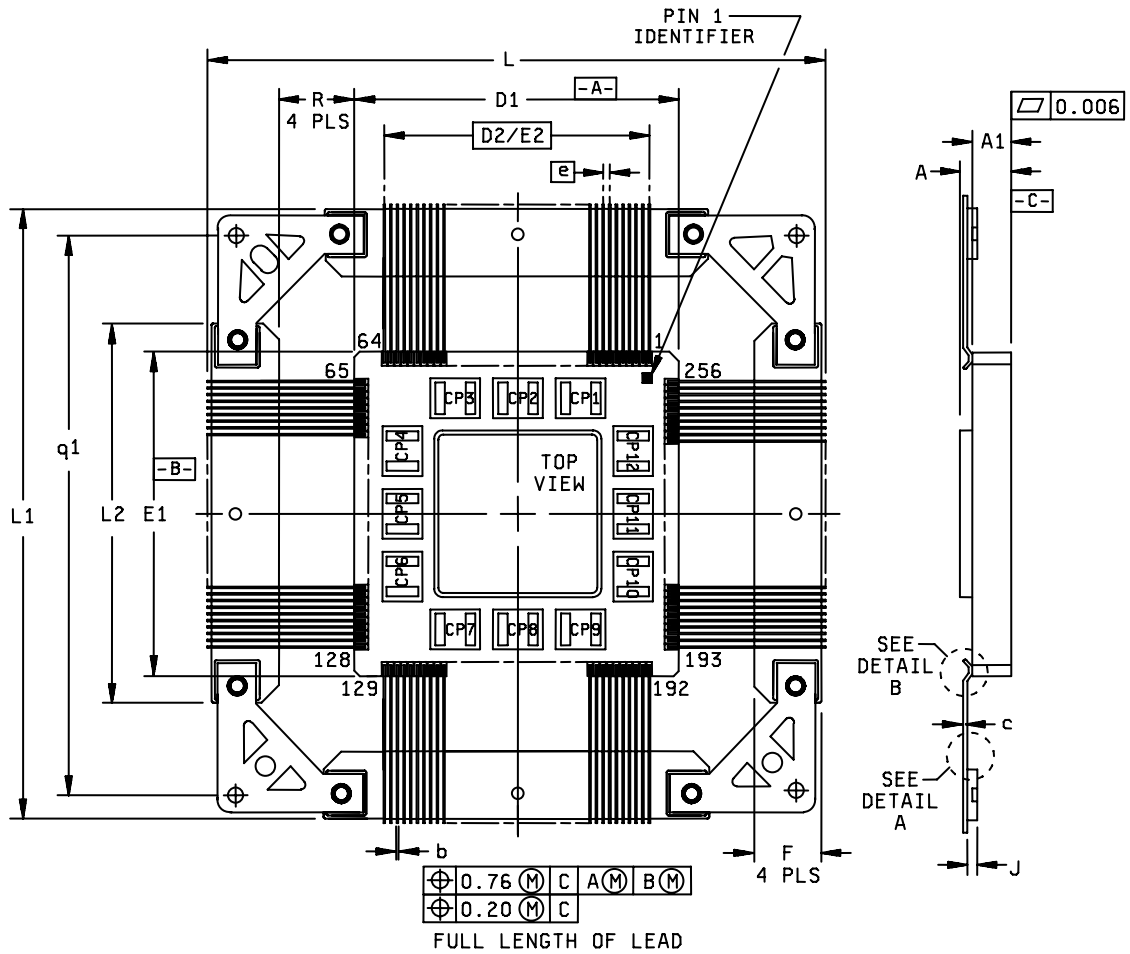


FIGURE 1. Case outline - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 12

Case Y - Continued

CP1	V _{DCCQ}	CP5	V _{DD1}	CP9	V _{DD1}
CP2	V _{DDNCQ}	CP6	V _{DD1}	CP10	V _{DD1}
CP3	V _{DD1}	CP7	V _{DD1}	CP11	V _{DD1}
CP4	V _{DD1}	CP8	V _{DD1}	CP12	V _{DCCQ}

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.68		.145
A1	2.46	3.02	.097	.119
A2		0.25		.010
A3		1.90		.074
A4	0.89 REF		.035 REF	
A5		0.89		.035
A6	1.27 REF		.050 REF	
B1		1.65		.065
B2		0.46		.018
b	0.15	0.25	.006	.010
c	0.10	0.20	.004	.008
e	0.50 BSC		.0197 BSC	
F		7.75		.306
D1/E1	35.64	36.36	1.403	1.431
D2/E2	31.50 BSC		1.240 BSC	
L		77.21		3.040
L1		75.39		2.953
L2	55.79	56.81	2.196	2.237
K1	1.524		.060	
K2	2.54		.100	
K3	3.556		.140	
K4	2.22		.087	
K5	1.40		.055	
q1		70.00		2.756
R	14.50		.570	
J	0.77	1.03	.030	.041

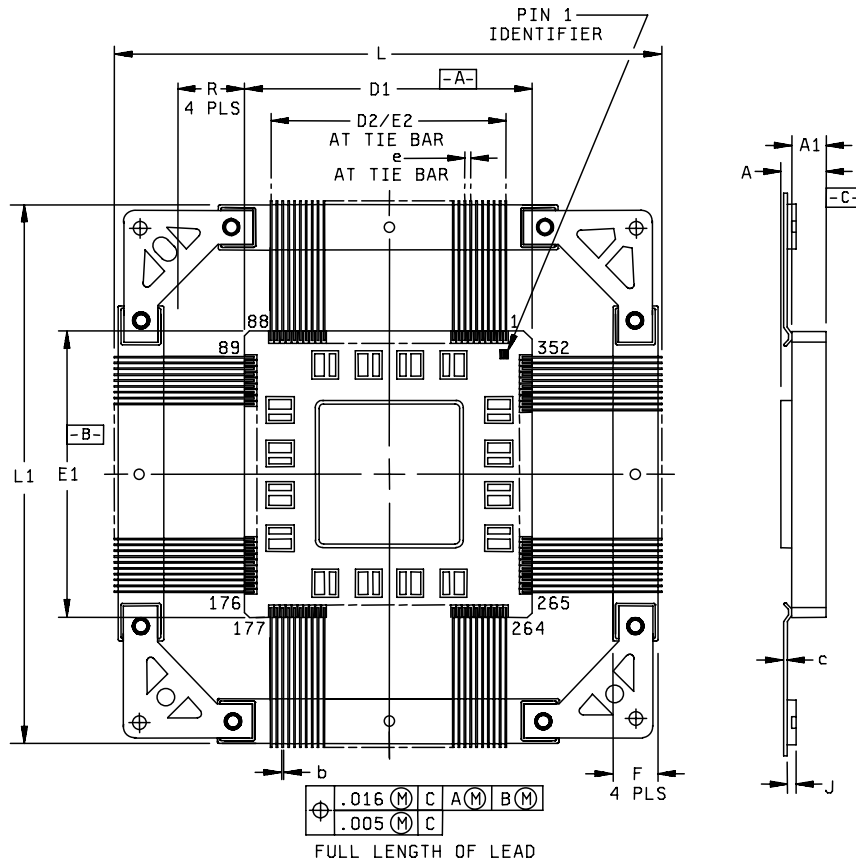
Notes:

1. All exposes metalized areas are gold plated over nickel plating.
2. The lid is connected to V_{SS}.
3. Capacitors pads are designed for a MIL-PRF-55681 CDR33BX, 50V .1μF chip cap.
4. Tiebar areas may have notches and tabs different than shown.
5. Packages may be shipped with repaired leads as shown. Coplanarity requirements do not apply in repaired areas.

FIGURE 1. Case outline - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 13

Case Z



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		3.35		.132	F	4.50	5.50	.177	.217
A1	2.90	3.25	.114	.128	R	7.95		.313	
c	0.10	0.20	.004	.008	J	0.77	1.03	.030	.041
e	0.50 BSC		.0197 BSC		L		77.21		3.040
D1/E1	47.52	48.48	1.871	1.909	L1		75.38		2.968
D2/E2	43.50 Basic		1.713 Basic						

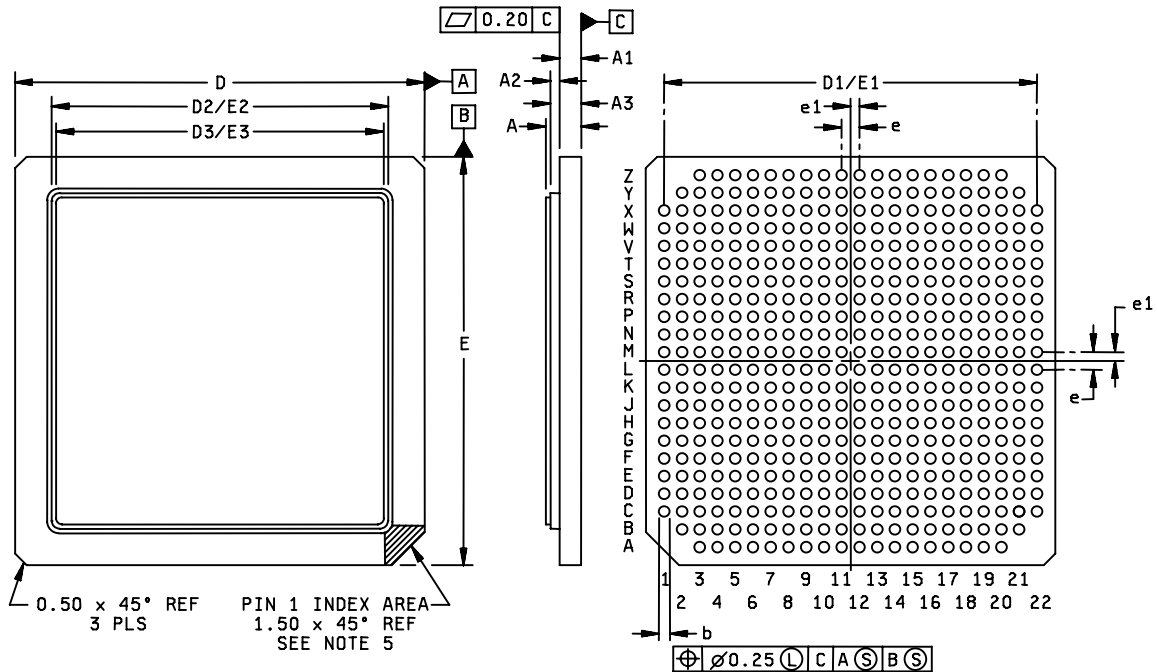
Notes:

1. Lead finish is in accordance with MIL-PRF-38535.
2. The lid is connected to V_{SS} .
3. Packages may be shipped with repaired leads as shown. Coplanarity requirements do not apply in repaired areas.
4. Package material: Opaque 90% minimum alumina ceramic.

FIGURE 1. Case outline - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 14

Case U



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.88	3.36	.113	.132
A1		2.18		.086
A2		0.81		.032
A3		3.01		.118
b	0.75	0.85	.030	.033
e	1.27 BSC		.050 BSC	
e1	0.63 BSC		.025 BSC	
D/E	28.71	29.29	1.130	1.153
D1/E1	26.67 Typ		1.050 Typ	
D2/E2	24.64	25.14	.970	.990
D3/E3	24.18	24.34	.952	.958

Notes:

1. Die attach and seal ring are connected to V_{SS} .
2. All exposed topside metallization areas are plated 100 to 225 microinches thick gold. Bottom side metallized areas are gold electro plated 60 microinches over electroplated nickel undercoating 100 to 350 microinches per MIL-PRF-38535.
3. Letter designations are for cross reference to MIL-STD-1835.
4. Geometry is vendor optional. Plating is optional.

FIGURE 1. Case outline - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 15

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device class Q and V, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device as described in the AID.
- c. Subgroup 4 (C_{IN} , C_{OUT} , and $C_{I/O}$ measurements) shall be measured only for initial qualification and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND. Capacitance testing shall be performed on three devices per Method 3012. A minimum of four pins per device shall be tested. Tested pins shall be selected based on engineering analysis of the package interconnect drawing to determine which pins will have the highest capacitance. The sample sizes may be increased based on engineering judgement, but shall not be decreased.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 16

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>2/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7	1, 7	1, 7
Group D end-point electrical parameters (see 4.4)	1, 7	1, 7	1, 7
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 17

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.5). SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or ≥ 10⁶ ions/cm².
- c. The flux shall be between 10² and 10⁵ ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The test temperature shall be as specified in Table IB SEP test limits.
- f. Bias conditions shall be defined by the manufacturer for latchup measurements.
- g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL B	SHEET 18

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Number of upsets (SEP).
- d. Number of transients (SEP).
- e. Occurrence of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-04B02
		REVISION LEVEL	SHEET 19

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-01-16

Approved sources of supply for SMD 5962-04B02 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1/</u> <u>2/</u>	Vendor CAGE number	Vendor Similar PIN <u>3/</u> <u>4/</u>
5962-04B0201Q_C <u>5/</u> 5962F04B0201V_C <u>5/</u>	65342	UT025RHD05
5962-04B0202Q_C <u>5/</u> 5962F04B0202V_C <u>5/</u>	65342	UT025RHD20
5962-04B0203Q_C <u>5/</u> 5962F04B0203V_C <u>5/</u>	65342	UT025RHD30

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Due to the nature of this SMD, the standard microcircuit drawing PIN and corresponding vendor similar PIN shall be specified in the AID. The vendor similar PIN will be based on the UT06MRA gate array family. Contact the listed approved source of supply for availability of case outlines (defined in 1.2.4) for each device.
- 3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 4/ Due to the manufacturer of this SMD, the standard microcircuit drawing PIN and corresponding vendor similar PIN shall be specified in the AID.
- 5/ Contact the listed approved source of supply for availability of case outlines (defined in 1.2.4) for each device.

Vendor CAGE
number

65342

Vendor name
and address

Aeroflex Colorado Springs Inc.
4350 Centennial Boulevard
Colorado Springs, CO 80907

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.