

AID No.

Version: A

Status:

1.0 SCOPE

1.1 Scope. This drawing defines specific requirements for DSCC Standard Military Drawing (SMD) 5962-96B02, Custom Application Specific Integrated Circuit (ASIC).

1.2 Identification. Identification shall be as follows:

Purchaser Part Number	Description	SMD Part Number	Manufacturer's Generic Part Number
	ASIC Custom Gate Array	5962R96B0208V4X	UT100E/R
	ASIC Custom Gate Array	5962R96B0208Q4X	UT100E/R
	Proto	NA	UT100E/R
	Commercial Space	NA	UT100E/R
	Reduced Hi-Rel	NA	UT100E/R

2.0 Applicable Document

2.1 Government Documents. The following documents from a part of this drawing to the extent specified herein. Unless otherwise specified, use the issue of these documents in effect at the start of processing.

DSCC SMD
5962-96B02 - Microcircuit, Digital, CMOS, Custom ASIC, Monolithic Silicon

2.2 Non-Government Publications

Controlled Test Media

XXXXXX - UTMC Design/Test CD-ROM
 XXXXXX - UTMC Design/Test CD-ROM
 XXXXXX - UTMC Design/Test CD-ROM
 XXXXXX - UTMC Test Program Tape
 30503/09 - UTMC Assembly and Test, Prototype Flowchart
 30503/06 - UTMC Assembly and Test, Reduced Hi-Rel Flowchart
 30503/03 - UTMC Assembly and Test, Commercial Space Flowchart

2.3 Order of Precedence. In the event of conflicts between documents, the requirements of this document shall take precedence.

3.0 Altered Item Drawing Requirements.

3.1 Terminal Connections, Pin Assignments and Functional Descriptions.

PIN	FUNCTION	I/O TYPE		PIN	FUNCTION	I/O TYPE
1	VDD	IN		2	VSS	IN
3				4		
5				6		
7				8		
9				10		
11				12		
13				14		
15				16		
17				18		

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19			20		OUT
21			22	VDDQ	IN
23	VSSQ	IN	24		
25			26		
27			28		
29			30		
31			32		
33			34		
35			36		
37			38		
39			40		
41			42	VDD	IN
43	VSS	IN	44		
45			46		
47			48		
49			50		
51			52		
53			54		
55			56		
57			58		
59			60		
61			62		
63	VDDQ	IN	64	VSSQ	IN
65	VDD	IN	66	VSS	IN
67			68		
69			70		
71			72		
73			74		
75			76		
77			78		
79			80		
81			82		
83			84		
85			86	VDDQ	IN
87	VSSQ	IN	88		
89			90		
91			92		
93			94		
95			96		
97			98		
99			100		
101			102		
103			104		
105			106	VDD	IN
107	VSS	IN	108		
109			110		
111			112		
113			114		
115			116		
117			118		
119			120		
121			122		

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PIN	FUNCTION	I/O TYPE		PIN	FUNCTION	I/O TYPE
123				124		
125				126		
127	VDDQ	IN		128	VSSQ	IN
129	VDD	IN		130	VSS	IN
131	VSS	IN		132		
133				134		
135				136		
137				138		
139				140		
141				142		
143				144		
145				146		
147				148		
149				150	VDDQ	IN
151	VSSQ	IN		152		
153				154		
155				156		
157				158		
159				160		
161				162		
163				164		
165				166		
167				168		
169				170	VDD	IN
171	VSS	IN		172		
173				174		
175				176		
177				178		
179				180		
181				182		
183				184		
185				186		
187				188		
189				190		
191	VDDQ	IN		192	VSSQ	IN
193	VDD	IN		194	VSS	IN
195				196		
197				198		
199				200		
201				202		
203				204		
205				206		
207				208		
209				210		
211				212		
213				214	VDDQ	IN

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215	VSSQ	IN		216		
217				218		
219				220		
221				222		
223				224		
225				226		
227				228		
229				230		
231				232		
233				234	VDD	IN
235	VSS	IN		236		
237				238		
239				240		
241				242		
243				244		
245				246		
247				248		
249				250		
251				252		
253				254		
255	VDDQ	IN		256	VSSQ	IN

3.2 Package Type.

XXXX – Outline Letter 4, 256 -Pin Flatpack (Paragraph 1.2.4 of 5962-96B02).

3.3 Functional Block Diagram. The functional block diagram is considered proprietary by XXX and is not part of this Altered Item Drawing.

3.4 Logic Diagram The logic diagram is defined in controlled CD-ROMs XXXXX-1, -2, and -3.

3.5 Pin Functional description. See 3.1

3.6 Design Document Name. The netlist is defined in controlled CD-ROMs XXXXX-1, -2, and -3.

3.7 Test Functional Tape. Test functional tape is in UTMIC's controlled test program 46-T505.

3.8 Switching Waveform. Switching waveforms are defined in Controlled CD-ROMs XXXXX-1, -2, and -3.

3.9 Fault Coverage. Fault coverage is ___% as achieved by Scan/ATPG vectors

3.10 Device Electrical Performance Characteristics. DC parameters are defined in 5962-96B02. AC parameters are defined in controlled CD-ROMs XXXXX-1, -2, and -3.

3.11 Maximum Power Dissipation. Maximum power dissipation is .803 Watts.

3.12 Burn-In Test Circuit. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in UTMIC's QM plan in accordance with MIL- PRF-38535. For Dynamic burn-in, UTMIC will use the scan check test vector pattern defined by the Synopsys test compiler during ATPG. This scan pattern meets UTMIC requirements for waveform type and vector count.

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3.13 Radiation Hardness Assurance. RHA lever designator R (100,000 Rad (Si)).

3.14 Device Class. The device class is Q.