

UT6325 RadTol Eclipse FPGA

Data Sheet

March 2010

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FEATURES

- ❑ 0.25 μ m, five-layer metal, ViaLink™ epitaxial CMOS process for smallest die sizes
- ❑ One-time programmable, ViaLink technology for personalization
- ❑ Typical performance characteristics -- 120 MHz 16-bit counters, 120 MHz datapaths, 60+ MHz FIFOs
- ❑ 2.5V core supply voltage, 3.3V I/O supply voltage
- ❑ Up to 320,000 system gates (non-volatile)
- ❑ I/Os
 - Interfaces with 3.3 volt
 - PCI compliant with 3.3 volt
 - Full JTAG 1149.1 compliant
 - Registered I/O cells with individually controlled enables
- ❑ Operational environment; total dose irradiation testing to MIL-STD-883 Test Method 1019
 - Total-dose: 300 krad(Si)
 - SEL Immune: >120MeV-cm²/mg
 - LET_{TH} (0.25) MeV-cm²/mg:
 - >42 logic cell flip flops
 - >64 for embedded SRAM
 - Saturated Cross Section (cm²) per bit
 - 5.0E-7 logic cell flip flops
 - 2.0E-7 embedded SRAM
- ❑ Up to 24 dual-port RadTol SRAM modules, organized in user-configurable 2,304 bit blocks
 - 5ns access times, each port independently accessible
 - Fast and efficient for FIFO, RAM, and initialized RAM functions
- ❑ 100% routable with full logic cell utilization and 100% user fixed I/O
- ❑ Variable-grain logic cells provide high performance and 100% utilization
- ❑ Typical logic utilization = 65-80% (design dependent)

- ❑ Comprehensive design tools include high quality Verilog/VHDL synthesis and simulation
- ❑ QuickLogic IP available for microcontrollers, DRAM controllers, USART and PCI
- ❑ Packaged in a 208-pin CQFP, 288 CQFP, 484 CCGA, 484 CLGA, 208 PQFP, 280 PBGA, and 484 PBGA
- ❑ Standard Microcircuit Drawing 5962-04229
 - QML Q & V

INTRODUCTION

The UT6325 RadTol Eclipse Field Programmable Gate Array Family (FPGA) offers up to 320,000 system gates including Dual-Port RadTol SRAM modules. It is fabricated on 0.25 μ m five-layer metal ViaLink CMOS process and contains 1,536 logic cells and 24 dual-port SRAM modules (see Figure 1 Block Diagram). Each SRAM module has 2,304 RAM bits, for a maximum total of 55,300 bits. Please reference product family features chart on page 2.

SRAM modules are Dual Port (one asynchronous/synchronous read port, one write port) and can be configured into one of four modes (see Figure 2). Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules (see Figure 3). This approach allows a variety of address depths and word widths to be tailored to a specific application.

The UT6325 RadTol Eclipse FPGA is available in a 208-pin Cerquad Flatpack, allowing access to 99 bidirectional signal I/O, 1 dedicated clock, 8 programmable clocks and 16 high drive inputs. Other package options include a 288 CQFP, 484 CCGA and a 484 CLGA.

Aeroflex uses QuickLogic Corporation's licensed ESP (Embedded Standard Products) technology. QuickLogic is a pioneer in the FPGA semiconductor and software tools field.

UT6325 Product Features

Features									
Device	System Gates	Logic Cells	Maximum Flip Flops	Logic Cell Flip Flops	RAM Modules	RAM Bits	I/O Standards	Clocks	High Drive Inputs
UT6325	320,640	1,536	4,002	3072	24	55,300	LVTTL, LVCMOS3, PCI	9	16

Operational Environment				
Device	Total Dose	LET _{TH} (0.25) MeV-cm ² /mg	Saturated Cross Section	Latch-up Immune
UT6325	3E5	>42 logic cell flip flops >64 embedded SRAM	5.0E-7 logic cell flip flops 2.0E-7 embedded SRAM	>120

Device	Bidirectional I/O per Package						
	208 PQFP	208 CQFP	280PBGA	288 CQFP	484 PBGA	484 CLGA	484 CCGA
UT6325	99	99	163	163	310	316	316

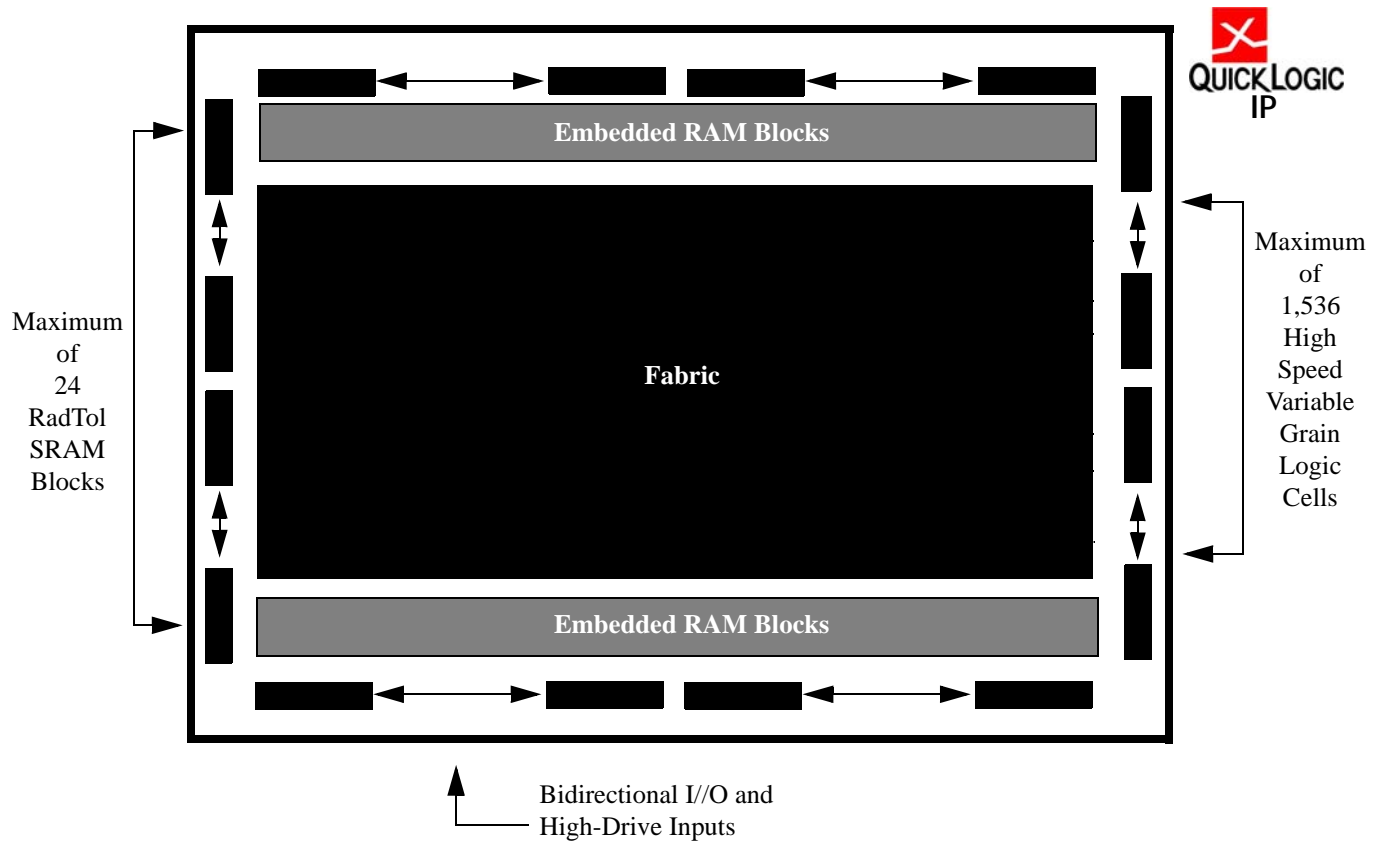


Figure 1. UT6325 Eclipse FPGA Block Diagram

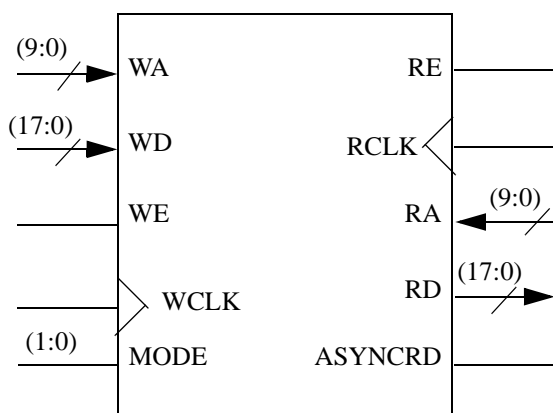


Figure 2. UT6325 Eclipse FPGA RAM Module

Software support for the product is available from both Aeroflex and QuickLogic. The Windows PC-based QuickWorks™ package provides the most complete software solution from design entry to logic synthesis, place and route, simulation, static timing, and power analysis. Device libraries are available to provide support for designers who use Mentor, Synplicity, Synopsys or other third party tools for design entry, synthesis and simulation. Please visit QuickLogic's website at www.quicklogic.com for more information.

The variable grain logic cell features up to 17 simultaneous inputs and 6 outputs within a cell that can be fragmented into 6 independent sections. Each cell has a fan-in of 30 including register and control lines (see Figure 5).

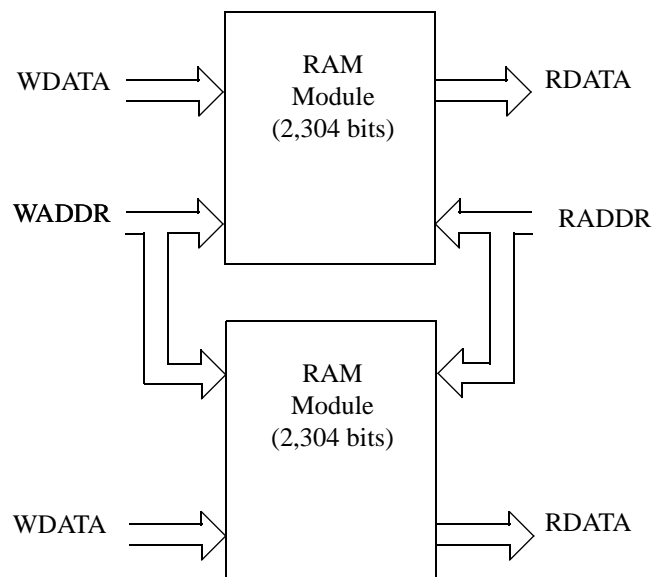


Figure 3. UT6325 Eclipse FPGA Module Bits

PRODUCT DESCRIPTION

I/O Pins

- Up to 316 bi-directional input/output pins, PCI-compliant for 3.3V buses (see Table 4)
- Each bidirectional I/O contains RadTol flip-flops for input, output, and output enable lines

Distributed Networks

- One, dedicated clock network, hardwired to each logic cell flip-flop clock pin to minimize skew
- Three programmable, global clock networks accessible from clock input only pins
- Five programmable quadrant clock networks, accessible from clock pins or internal logic
- 20 pre-defined Quad-clock networks, five per quadrant. Accessed by the five programmable quadrant clock networks
- Sixteen high drive inputs. Two inputs located in each of the eight I/O banks. Used as clock or enable signals for the I/O RadTol flip-flops, or as high drive inputs for internal logic

Typical Performance

- Input + logic cell + output total delays under 12ns
- Data path speeds over 120 MHz
- Counter speeds over 120 MHz
- FIFO speeds over 60+ MHz

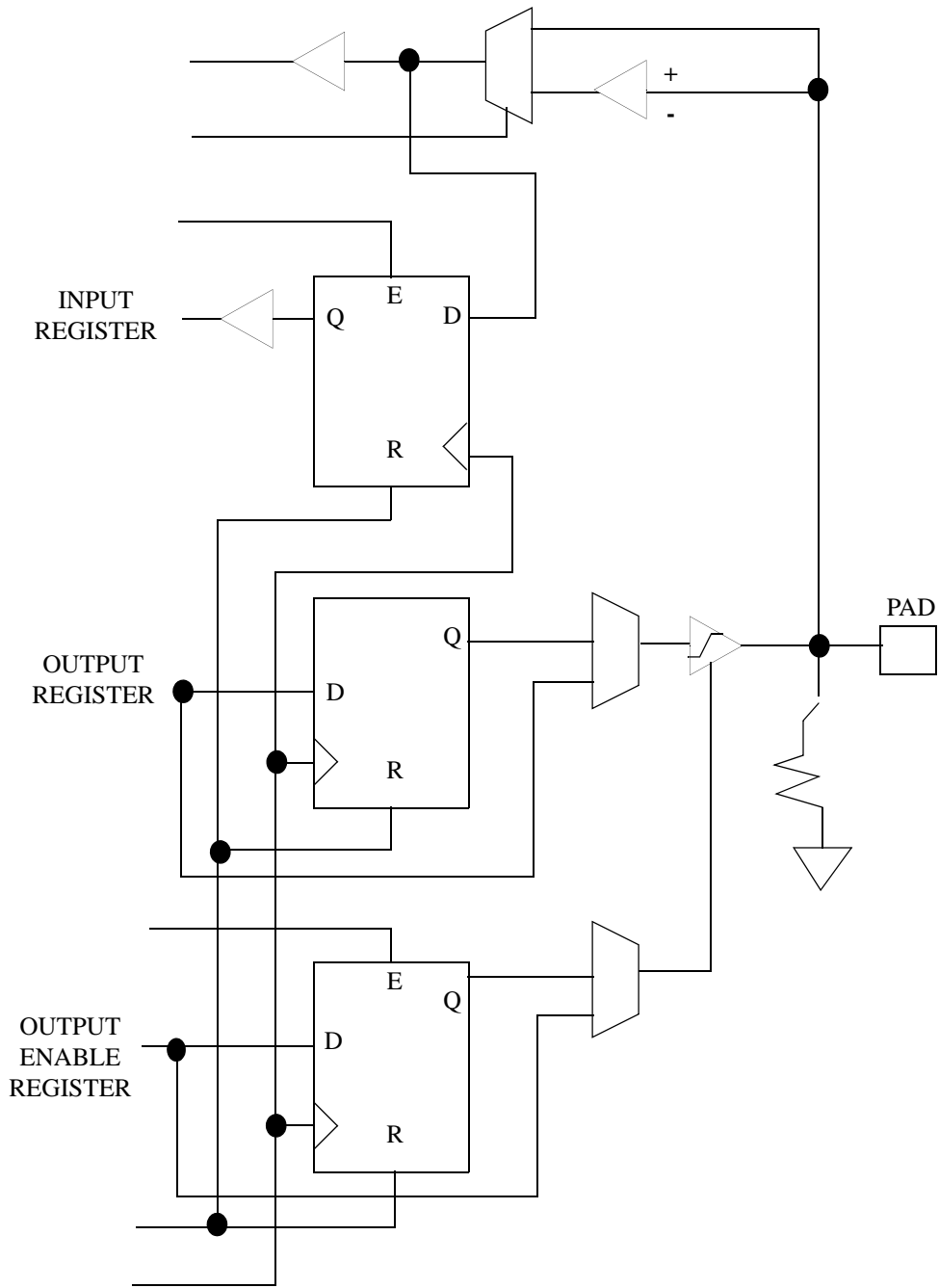


Figure 4. RadTol Eclipse FPGA I/O Cell

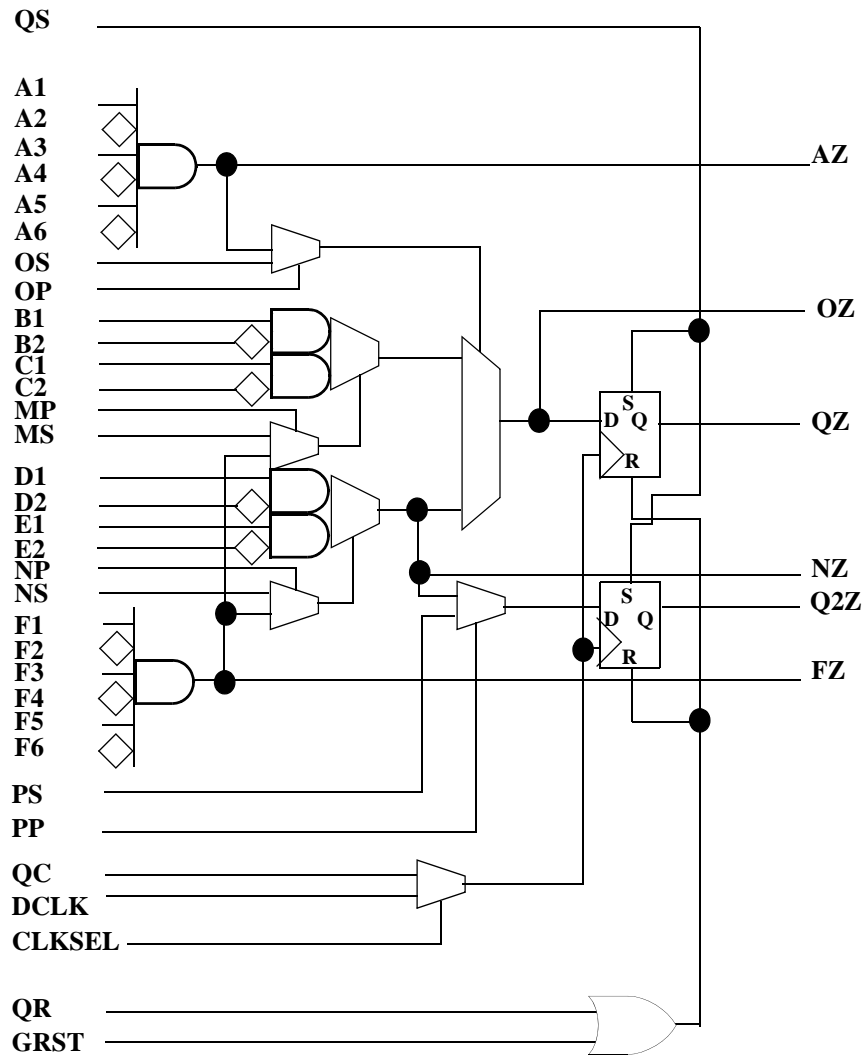


Figure 5. RadTol Eclipse FPGA Logic Cell

Table 1: 208-pin Ceramic Quad Flatpack Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	PLL RST(3)	36	IO(B)	71	IO(C)	106	V _{CCPLL} (1)	141	IO(F)	176	IO(G)
2	V _{CCPLL} (3)	37	IO(B)	72	V _{CCIO} (C)	107	IO(E)	142	IO(F)	177	V _{CCIO} (G)
3	GND	38	IO(B)	73	IO(C)	108	GND	143	IO(F)	178	GND
4	GND	39	IOCTRL(B)	74	IO(C)	109	IO(E)	144	IOCTRL(F)	179	IO(G)
5	IO(A)	40	INREF(B)	75	GND	110	IO(E)	145	INREF(F)	180	IO(G)
6	IO(A)	41	IOCTRL(B)	76	V _{CC}	111	V _{CCIO} (E)	146	V _{CC}	181	IO(G)
7	IO(A)	42	IO(B)	77	IO(C)	112	IO(E)	147	IOCTRL(F)	182	V _{CC}
8	V _{CCIO} (A)	43	IO(B)	78	TRSTB	113	V _{CC}	148	IO(F)	183	TCK
9	IO(A)	44	V _{CCIO} (B)	79	V _{CC}	114	IO(E)	149	IO(F)	184	V _{CC}
10	IO(A)	45	IO(B)	80	IO(D)	115	IO(E)	150	V _{CCIO} (F)	185	IO(H)
11	IOCTRL(A)	46	V _{CC}	81	IO(D)	116	IO(E)	151	IO(F)	186	IO(H)
12	V _{CC}	47	IO(B)	82	IO(D)	117	IOCTRL(E)	152	IO(F)	187	IO(H)
13	INREF(A)	48	IO(B)	83	GND	118	INREF(E)	153	GND	188	GND
14	IOCTRL(A)	49	GND	84	V _{CCIO} (D)	119	IOCTRL(E)	154	IO(F)	189	V _{CCIO} (H)
15	IO(A)	50	TDO	85	IO(D)	120	IO(E)	155	PLLOUT(3)	190	IO(H)
16	IO(A)	51	PLLOUT(1)	86	V _{CC}	121	IO(E)	156	GNDPLL(0)	191	IO(H)
17	IO(A)	52	GNDPLL(2)	87	IO(D)	122	V _{CCIO} (E)	157	GND	192	IOCTRL(H)
18	IO(A)	53	GND	88	IO(D)	123	GND	158	V _{CCPLL} (0)	193	IO(H)
19	V _{CCIO} (A)	54	V _{CCPLL} (2)	89	V _{CC}	124	IO(E)	159	PLL RST(0)	194	INREF(H)
20	IO(A)	55	PLL RST(2)	90	IO(D)	125	IO(E)	160	GND	195	V _{CC}
21	GND	56	V _{CC}	91	IO(D)	126	IO(E)	161	IO(G)	196	IOCTRL(H)
22	IO(A)	57	IO(C)	92	IOCTRL(D)	127	CLK(5) PLLIN(3)	162	V _{CCIO} (G)	197	IO(H)
23	TDI	58	GND	93	INREF(D)	128	CLK(6)	163	IO(G)	198	IO(H)
24	CLK(0)	59	IO(C)	94	IOCTRL(D)	129	V _{CC}	164	IO(G)	199	IO(H)
25	CLK(1)	60	V _{CCIO} (C)	95	IO(D)	130	CLK(7)	165	V _{CC}	200	IO(H)
26	V _{CC}	61	IO(C)	96	IO(D)	131	V _{CC}	166	IO(G)	201	IO(H)
27	CLK(2) PLLIN(2)	62	IO(C)	97	IO(D)	132	CLK(8)	167	IO(G)	202	IO(H)
28	CLK(3) PLLIN(1)	63	IO(C)	98	V _{CCIO} (D)	133	TMS	168	IO(G)	203	V _{CCIO} (H)
29	V _{CC}	64	IO(C)	99	IO(D)	134	IO(F)	169	IOCTRL(G)	204	GND
30	CLK(4), DEDCLK PLLIN(0)	65	IO(C)	100	IO(D)	135	IO(F)	170	INREF(G)	205	IO(H)
31	IO(B)	66	IO(C)	101	GND	136	IO(F)	171	IOCTRL(G)	206	PLLOUT(2)
32	IO(B)	67	IOCTRL(C)	102	PLLOUT(0)	137	GND	172	IO(G)	207	GND
33	GND	68	INREF(C)	103	GND	138	V _{CCIO} (F)	173	IO(G)	208	GNDPLL(3)
34	V _{CCIO} (B)	69	IOCTRL(C)	104	GNDPLL(1)	139	IO(F)	174	IO(G)		
35	IO(B)	70	IO(C)	105	PLL RST(1)	140	IO(F)	175	V _{CC}		

Table 2: 288-pin Ceramic Quad Flatpack Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	GND	36	CLK(7)	71	V _{CC}	106	IO(G)	141	PLLST(3)	176	IO(A)
2	V _{CC}	37	CLK(8)	72	GND	107	TCK	142	V _{CC} PLL(3)	177	TDI
3	PLLST(1)	38	TMS	73	GND	108	V _{CC}	143	V _{CC}	178	CLK(0)
4	V _{CC} PLL(1)	39	IO(F)	74	V _{CC}	109	IO(H)	144	GND	179	CLK(1)
5	IO(E)	40	IO(F)	75	GND	110	IO(H)	145	GND	180	CLK(2) PLLIN(2)
6	IO(E)	41	IO(F)	76	PLLST(0)	111	IO(H)	146	V _{CC}	181	CLK(3) PLLIN(1)
7	IO(E)	42	IO(F)	77	IO(F)	112	IO(H)	147	GND	182	CLK(4), DEDCLK, PLLIN(0)
8	IO(E)	43	V _{CC}	78	IO(F)	113	IO(H)	148	IO(A)	183	IO(B)
9	IO(E)	44	GND	79	IO(F)	114	IO(H)	149	IO(A)	184	IO(B)
10	IO(E)	45	V _{CC} IO(F)	80	IO(G)	115	V _{CC}	150	IO(A)	185	IO(B)
11	IO(E)	46	IO(F)	81	IO(G)	116	GND	151	IO(A)	186	IO(B)
12	IO(E)	47	IO(F)	82	IO(G)	117	V _{CC} IO(H)	152	IO(A)	187	V _{CC}
13	IO(E)	48	IO(F)	83	IO(G)	118	IO(H)	153	IO(A)	188	GND
14	V _{CC}	49	IO(F)	84	IO(G)	119	IO(H)	154	IO(A)	189	V _{CC} IO(B)
15	GND	50	IO(F)	85	IO(G)	120	IO(H)	155	IO(A)	190	IO(B)
16	V _{CC} IO(E)	51	IO(F)	86	V _{CC}	121	IOCTRL(H)	156	IOCTRL(A)	191	IO(B)
17	IOCTRL(E)	52	INREF(F)	87	GND	122	IO(H)	157	INREF(A)	192	IO(B)
18	INREF(E)	53	IOCTRL(F)	88	V _{CC} IO(G)	123	INREF(H)	158	V _{CC}	193	IO(B)
19	IOCTRL(E)	54	IOCTRL(F)	89	IO(G)	124	IOCTRL(H)	159	GND	194	IO(B)
20	IO(E)	55	IO(F)	90	IOCTRL(G)	125	IO(H)	160	V _{CC} IO(A)	195	IOCTRL(B)
21	IO(E)	56	IO(F)	91	INREF(G)	126	IO(H)	161	IOCTRL(A)	196	INREF(B)
22	IO(E)	57	V _{CC} IO(F)	92	IOCTRL(G)	127	IO(H)	162	IO(A)	197	IOCTRL(B)
23	IO(E)	58	GND	93	IO(G)	128	IO(H)	163	IO(A)	198	IO(B)
24	IO(E)	59	V _{CC}	94	IO(G)	129	V _{CC} IO(H)	164	IO(A)	199	IO(B)
25	IO(E)	60	IO(F)	95	IO(G)	130	GND	165	IO(A)	200	IO(B)
26	IO(E)	61	IO(F)	96	IO(G)	131	V _{CC}	166	IO(A)	201	V _{CC} IO(B)
27	IO(E)	62	IO(F)	97	IO(G)	132	IO(H)	167	IO(A)	202	GND
28	V _{CC} IO(E)	63	IO(F)	98	IO(G)	133	IO(H)	168	IO(A)	203	V _{CC}
29	GND	64	IO(F)	99	IO(G)	134	IO(H)	169	IO(A)	204	IO(B)
30	V _{CC}	65	IO(F)	100	V _{CC} IO(G)	135	IO(A)	170	IO(A)	205	IO(B)
31	IO(E)	66	IO(F)	101	GND	136	IO(A)	171	IO(A)	206	IO(B)
32	IO(E)	67	IO(F)	102	V _{CC}	137	IO(A)	172	V _{CC} IO(A)	207	IO(B)
33	IO(E)	68	PLLOUT(3)	103	IO(G)	138	PLLOUT(2)	173	GND	208	IO(B)
34	CLK(5) PLLIN(3)	69	GNDPLL(0)	104	IO(G)	139	GND	174	V _{CC}	209	IO(B)
35	CLK(6)	70	V _{CC} PLL(0)	105	IO(G)	140	GNDPLL(3)	175	IO(A)	210	IO(B)

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
211	TDO	224	IO(B)	237	IOCTRL(C)	250	IO(C)	263	IO(D)	276	IO(D)
212	PLLOUT(1)	225	IO(C)	238	INREF(C)	251	IO(C)	264	IO(D)	277	IO(D)
213	GNDPLL(2)	226	IO(C)	239	IOCTRL(C)	252	TRSTB	265	IO(D)	278	IO(D)
214	IO(B)	227	IO(C)	240	IO(C)	253	V _{CC}	266	IO(D)	279	IO(D)
215	V _{CC}	228	IO(C)	241	IO(C)	254	IO(D)	267	IO(D)	280	IO(D)
216	GND	229	IO(C)	242	IO(C)	255	IO(D)	268	IO(D)	281	IO(E)
217	GND	230	V _{CC}	243	IO(C)	256	IO(D)	269	IO(D)	282	IO(E)
218	V _{CC}	231	GND	244	V _{CCIO} (C)	257	IO(D)	270	IOCTRL(D)	283	IO(E)
219	GND	232	V _{CCIO} (C)	245	GND	258	IO(D)	271	INREF(D)	284	PLLOUT(0)
220	V _{CCPLL} (2)	233	IO(C)	246	V _{CC}	259	V _{CC}	272	IOCTRL(D)	285	GND
221	PLLRST(2)	234	IO(C)	247	IO(C)	260	GND	273	V _{CCIO} (D)	286	GNDPLL(1)
222	IO(B)	235	IO(C)	248	IO(C)	261	V _{CCIO} (D)	274	GND	287	V _{CC}
223	IO(B)	236	IO(C)	249	IO(C)	262	IO(D)	275	V _{CC}	288	GND

Table 3: 484-pin Ceramic Land Grid Array and Plastic Ball Grid Array Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	IO(A)	AA14	IO(D)	B5	IO(A)	C18	IO(G)	E9	IO(H)	F22	IOCTRL(F)
A2	PLLST(3)	AA15	IO(D)	B6	IO(H)	C19	IO(F)	E10	IO(H)	G1	IO(A)
A3	IO(A)	AA16	IO(D)	B7	IO(H)	C20	GNDPLL(0)	E11	V _{CC}	G2	IO(A)
A4	IO(A)	AA17	IO(D)	B8	INREF(H)	C21	IO(F)	E12	IO(G)	G3	IO(A)
A5	IO(A)	AA18	IO(D)	B9	IO(H)	C22	IO(F)	E13	IO(G)	G4	IO(A)
A6	IO(H)	AA19	IO(E)	B10	IO(H)	D1	IO(A)	E14	IO(G)	G5	IO(A)
A7	IO(H)	AA20	GNDPLL(1)	B11	IO(H)	D2	IO(A)	E15	IOCTRL(G)	G6	IO(A)
A8	IOCTRL(H)	AA21	IO(E)	B12	NC	D3	IO(A)	E16	IO(G)	G7	GND
A9	IO(H)	AA22	IO(E)	B13	NC	D4	IO(A)	E17	INREF(G)	G8	IO(H)
A10	NC	AB1	IO(B)	B14	NC	D5	IO(A)	E18	IO(G)	G9	IO(H)
A11	IO(H)	AB2	GNDPLL(2)	B15	IO(G)	D6	IO(H)	E19	IO(F)	G10	IO(H)
A12	TCK	AB3	PLLST(2)	B16	IO(G)	D7	IO(H)	E20	IO(F)	G11	IO(G)
A13	IO(G)	AB4	IO(B)	B17	IO(G)	D8	IO(H)	E21	IO(F)	G12	GND
A14	IO(G)	AB5	IO(B)	B18	IO(G)	D9	IO(H)	E22	IO(F)	G13	IO(G)
A15	IO(G)	AB6	IO(C)	B19	PLLST(0)	D10	IO(H)	F1	IO(A)	G14	IO(G)
A16	IO(G)	AB7	IO(C)	B20	IO(F)	D11	IO(H)	F2	INREF(A)	G15	IO(G)
A17	IO(G)	AB8	IOCTRL(C)	B21	IO(F)	D12	IO(G)	F3	IO(A)	G16	GND
A18	IO(G)	AB9	IO(C)	B22	IO(F)	D13	IO(G)	F4	IO(A)	G17	V _{CCIO} (F)
A19	IO(F)	AB10	IO(C)	C1	IO(A)	D14	IO(G)	F5	IO(A)	G18	IO(F)
A20	GND	AB11	IO(C)	C2	IO(A)	D15	IOCTRL(G)	F6	V _{CCIO} (A)	G19	IO(F)
A21	PLLOUT(3)	AB12	IO(D)	C3	V _{CCPLL} (3)	D16	IO(G)	F7	V _{CCIO} (H)	G20	IO(F)
A22	IO(F)	AB13	IO(D)	C4	PLLOUT(2)	D17	IO(G)	F8	IO(H)	G21	INREF(F)
AA1	TDO	AB14	IO(D)	C5	IO(A)	D18	IO(F)	F9	V _{CCIO} (H)	G22	IO(F)
AA2	PLLOUT(1)	AB15	IO(D)	C6	IO(H)	D19	V _{CCPLL} (0)	F10	IO(H)	H1	IO(A)
AA3	GND	AB16	IOCTRL(D)	C7	IO(H)	D20	IO(F)	F11	V _{CCIO} (H)	H2	IO(A)
AA4	IO(B)	AB17	IO(D)	C8	IO(H)	D21	IO(F)	F12	V _{CCIO} (G)	H3	IO(A)
AA5	IO(C)	AB18	IO(D)	C9	IOCTRL(H)	D22	IO(F)	F13	IO(G)	H4	IO(A)
AA6	IO(C)	AB19	IO(E)	C10	IO(H)	E1	IOCTRL(A)	F14	V _{CCIO} (G)	H5	IOCTRL(A)
AA7	IO(C)	AB20	GND	C11	IO(H)	E2	IO(A)	F15	NC	H6	V _{CCIO} (A)
AA8	INREF(C)	AB21	V _{CCPLL} (1)	C12	IO(H)	E3	IO(A)	F16	V _{CCIO} (G)	H7	IO(H)
AA9	IO(C)	AB22	IO(E)	C13	IO(G)	E4	IO(A)	F17	IO(F)	H8	GND
AA10	IO(C)	B1	IO(A)	C14	IO(G)	E5	IO(A)	F18	IO(F)	H9	V _{CC}
AA11	IO(C)	B2	GND	C15	IO(G)	E6	IO(H)	F19	IO(F)	H10	V _{CC}
AA12	IO(D)	B3	GNDPLL(3)	C16	IO(G)	E7	IO(A)	F20	IOCTRL(F)	H11	V _{CC}
AA13	IO(D)	B4	GND	C17	IO(G)	E8	IO(H)	F21	IO(F)	H12	GND

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
H13	V _{CC}	K4	IO(A)	L17	V _{CCIO} (F)	N8	V _{CC}	P21	IO(E)	T12	IO(C)
H14	V _{CC}	K5	IO(A)	L18	IO(F)	N9	V _{CC}	P22	IO(E)	T13	IO(D)
H15	GND	K6	V _{CCIO} (A)	L19	CLK(8)	N10	GND	R1	IO(B)	T14	IO(E)
H16	IO(F)	K7	IO(A)	L20	IO(F)	N11	GND	R2	INREF(B)	T15	IO(D)
H17	IO(F)	K8	V _{CC}	L21	IO(F)	N12	GND	R3	IO(B)	T16	GND
H18	IO(F)	K9	V _{CC}	L22	IO(F)	N13	GND	R4	IO(B)	T17	IO(E)
H19	IO(F)	K10	GND	M1	IO(B)	N14	V _{CC}	R5	IO(B)	T18	IO(E)
H20	IO(F)	K11	GND	M2	IO(B)	N15	V _{CC}	R6	IO(B)	T19	IO(E)
H21	IO(F)	K12	GND	M3	IO(B)	N16	IO(E)	R7	IO(B)	T20	IO(E)
H22	IO(F)	K13	GND	M4	CLK(3) PLLIN(1)	N17	V _{CCIO} (E)	R8	GND	T21	IOCTRL(E)
J1	IO(A)	K14	V _{CC}	M5	IO(B)	N18	IO(E)	R9	V _{CC}	T22	IO(E)
J2	IO(A)	K15	V _{CC}	M6	V _{CCIO} (B)	N19	IO(E)	R10	V _{CC}	U1	IOCTRL(B)
J3	IO(A)	K16	IO(F)	M7	CLK(1)	N20	IO(E)	R11	GND	U2	IO(B)
J4	IO(A)	K17	IO(F)	M8	V _{CC}	N21	IO(E)	R12	V _{CC}	U3	IOCTRL(B)
J5	IO(A)	K18	IO(F)	M9	V _{CC}	N22	IO(E)	R13	V _{CC}	U4	IO(B)
J6	IO(A)	K19	IO(F)	M10	GND	P1	IO(B)	R14	V _{CC}	U5	IO(B)
J7	IO(A)	K20	IO(F)	M11	GND	P2	IO(B)	R15	GND	U6	IO(C)
J8	V _{CC}	K21	IO(F)	M12	GND	P3	IO(B)	R16	IO(D)	U7	V _{CCIO} (C)
J9	GND	K22	IO(F)	M13	GND	P4	IO(B)	R17	V _{CCIO} (E)	U8	NC
J10	V _{CC}	L1	CLK4, DEDCLK PLLIN(0)	M14	GND	P5	IO(B)	R18	IO(E)	U9	V _{CCIO} (C)
J11	V _{CC}	L2	CLK(0)	M15	GND	P6	V _{CCIO} (B)	R19	IO(E)	U10	IO(C)
J12	GND	L3	CLK(2) PLLIN(2)	M16	GND	P7	IO(B)	R20	IO(E)	U11	V _{CCIO} (C)
J13	V _{CC}	L4	IO(A)	M17	IO(E)	P8	V _{CC}	R21	IO(E)	U12	V _{CCIO} (D)
J14	GND	L5	IO(A)	M18	IO(E)	P9	GND	R22	IO(E)	U13	IO(D)
J15	V _{CC}	L6	IO(A)	M19	IO(E)	P10	V _{CC}	T1	IO(B)	U14	V _{CCIO} (D)
J16	IO(F)	L7	GND	M20	CLK(7)	P11	GND	T2	IO(B)	U15	NC
J17	V _{CCIO} (F)	L8	GND	M21	CLK(5) PLLIN(3)	P12	V _{CC}	T3	IO(B)	U16	V _{CCIO} (D)
J18	IO(F)	L9	GND	M22	TMS	P13	V _{CC}	T4	IO(B)	U17	V _{CCIO} (E)
J19	IO(F)	L10	GND	N1	IO(B)	P14	GND	T5	IO(B)	U18	IO(E)
J20	IO(F)	L11	GND	N2	IO(B)	P15	V _{CC}	T6	V _{CCIO} (B)	U19	IO(E)
J21	IO(F)	L12	GND	N3	IO(B)	P16	IO(E)	T7	GND	U20	IOCTRL(E)
J22	IO(F)	L13	GND	N4	IO(B)	P17	IO(E)	T8	IO(C)	U21	IO(E)
K1	TDI	L14	V _{CC}	N5	IO(B)	P18	IO(E)	T9	IO(B)	U22	INREF(E)
K2	IO(A)	L15	V _{CC}	N6	IO(B)	P19	IO(E)	T10	TRSTB	V1	IO(B)
K3	IO(A)	L16	CLK(6)	N7	IO(B)	P20	IO(E)	T11	GND	V2	IO(B)

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
V3	IO(B)	V14	IO(D)	W3	IO(B)	W14	IO(D)	Y3	V _{CCPLL(2)}	Y14	IO(D)
V4	IO(B)	V15	IO(D)	W4	IO(B)	W15	IO(D)	Y4	IO(C)	Y15	IOCTRL(D)
V5	IO(B)	V16	INREF(D)	W5	IO(B)	W16	NC	Y5	IO(C)	Y16	IO(D)
V6	IO(C)	V17	IO(D)	W6	IO(C)	W17	IO(D)	Y6	IO(C)	Y17	IO(D)
V7	IO(C)	V18	IO(E)	W7	NC	W18	IO(E)	Y7	IO(C)	Y18	IO(E)
V8	IO(C)	V19	IO(E)	W8	IO(C)	W19	IO(E)	Y8	IOCTRL(C)	Y19	PLLOUT(0)
V9	NC	V20	IO(E)	W9	IO(C)	W20	IO(E)	Y9	IO(C)	Y20	PLLRST(1)
V10	IO(C)	V21	IO(E)	W10	IO(C)	W21	IO(E)	Y10	IO(C)	Y21	ID(E)
V11	IO(C)	V22	IO(E)	W11	IO(C)	W22	IO(E)	Y11	IO(D)	Y22	IO(E)
V12	V _{CC}	W1	IO(B)	W12	IO(D)	Y1	IO(B)	Y12	IO(D)		
V13	NC	W2	IO(B)	W13	IO(D)	Y2	IO(B)	Y13	IO(D)		

Table 4: UT6325 Eclipse FPGA Pin Description

PIN	FUNCTION	DESCRIPTION
TDI/RSI	Test data in for JTAG/RAM initialization Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to VCC if unused.
TRSTB/RRO	Active low reset for JTAG/RAM initialization reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused.
TMS	Test mode select for JTAG	Hold HIGH during normal operation. Connect to VCC if not used for JTAG.
TCK	Test clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCC or ground if not used for JTAG.
TDO/RCO	Test data out for JTAG/RAM initialization clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization.
CLK ¹	Global clock network driver	Low skew global clock. This pin provides access to a programmable clock network.
IO(A)	Input/Output Pin	The I/O pin is a bi-directional pin, configurable to input and/or output. The A inside the parenthesis means that the I/O is located in Bank A.
DEDCLK ¹	Dedicated clock pin	Low skew global clock. This pin provides access to a dedicated, distributed clock network capable of driving the CLOCK inputs of sequential elements of the device (e.g., RAM and flip-flops).
PLLIN ¹	PLL clock input	Clock input for PLL.
V _{CCPLL} ¹	Phase locked loop power supply pin	Voltage supply for PLLIN. V _{CCPLL} should be connected to 2.5V supply if the PLLs are used. If the PLLs are not used, V _{CCPLL} can be connected GND.
GNDPLL	Ground pin for PLL	Connect to GND.
PLL _{RST} ¹	Reset input pin for PLL	Reset input for PLL. If PLLs are not used, PLL _{RST} should be connect to the same voltage as V _{CCPLL} (e.g., GND).
PLL _{OUT} ²	PLL output pin	Dedicated PLL output pin. If PLLs are not used, PLL _{OUT} should be connected to GND.
INREF(A)	Differential reference voltage	The INREF is the reference voltage pin for GTL+, SSTL2, and STTL3 standards. The A inside the parenthesis means that INREF is located in Bank A. This pin should be tied to GND for LVTTTL, LVCMOS3 and PCI inputs.
IOCTRL(A) ¹	Highdrive input	This pin provides fast RESET, SET, CLOCK and ENABLE access to the I/O cell flip flops, providing fast clock-to-out and fast I/O response times. This pin can also double as a high-drive pin to the internal logic cells. The A inside the parenthesis means that IOCTRL is located in Bank A.
V _{CC}	Power supply pin	Connect to 2.5V supply.

Table 4: UT6325 Eclipse FPGA Pin Description

PIN	FUNCTION	DESCRIPTION
$V_{CCIO}(A)$	Input voltage tolerance pin	Connect to 3.3V supply. The A inside the parenthesis means that V_{CCIN} is located in Bank A. Every I/O pin in Bank A will be tolerance of V_{CCIO} input signals and will output V_{CCIO} level signals.
GND	Ground pin	Connect to ground.

Note: Four PLL inputs are available on the RadTol Eclipse FPGA. These PLL pins are noted and available in the QuickWorks/SpDE place and route tools. Aeroflex has tested and characterized the PLL circuits for jitter performance vs frequency and SEE. Aeroflex cautions against the use of the PLL circuits without a full review of the test results. Please contact Aeroflex Colorado Springs directly for support.

1. All dedicated inputs including the CLK, DEDCLK, PLLIN, PLLRST, and IOCTRL pins, are LVC MOS2 compliant (2.5V). Modifications to the ESD protection networks allow these pins to be driven up to $V_{CCIO} + 0.3V$. Slightly lower noise margins exist for these LVC MOS2 compliant inputs, as compared to the LVC MOS3 compliant bidirectional I/O.
2. All PLLOUT output pins are driven by the V_{CC} rail, not the V_{CCIO} rail. These output pins are LVC MOS2 compliant only (2.5V).

ABSOLUTE MAXIMUM RATINGS¹
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V _{CC}	Core supply voltage	-0.5 to 3.6V
V _{CCIO}	I/O supply voltage	-0.5 to 4.6V
V _{IO}	Voltage on any pin	-0.5V to V _{CCIO} +0.5V
I _{LU}	Electrical Latchup Immunity	+/-100mA
P _D	Power Dissipation	.5 - 2.5W
Θ _{JC}	Thermal resistance, junction-to-case ²	6°C/W
T _J	Maximum junction temperature ²	+150°C
ESDS	ESD pad protection	+/-2000V
I _I	DC input current	±10 mA
T _{LS}	Lead Temperature	300°C

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Test per MIL-STD-883; Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V _{CC}	Core supply voltage	2.3 to 2.7V
V _{CCIO}	I/O Input Tolerance Voltage	3.0 to 3.6V
T _A	Ambient Temperature	-55°C to +125°C
K ¹	Delay factor for FPGA	0.42 to 1.92 (speed grade -4)
t _{INRISE} t _{INFALL}	Maximum input rise or fall time (V _{IN} transitioning between V _{IL} (max) and V _{IH} (min))	20ns

Notes:

1. To conclude best and worst case delays, multiply the K factor from the operating conditions with the delay values defined in the following AC delay tables.

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*(-55°C to +125°C) ($2.3V \leq V_{CC} \leq 2.7V$)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
I_{IN1}	Input or I/O leakage current, all I/O except TRSTB, TDI, TMS	$V_{IN} = V_{CCIO}$ or Gnd	-2	2	μA
I_{IN2}	Input leakage current TRSTB, TDI, TMS	$V_{IN} = V_{CCIO}$ or Gnd	-20	5	μA
I_{IN2}	Input leakage current TRSTB, TDI, TMS post 300 krads(Si)	$V_{IN} = V_{CCIO}$ or Gnd	-50	50	μA
I_{OZ}	Three-state output leakage current	$V_{IN} = V_{CCIO}$ or Gnd	-10	10	μA
C_I^1	Input capacitance	--	-	8	pF
$C_{I/O}^1$	Bi-directional capacitance	--	-	12	pF
I_{OS}^2	Short-circuit output current	$V_O = GND$ $V_O = V_{CCIO}$	-15 40	-180 210	mA mA
I_{CC}^3	Core quiescent current	$V_{CC} = 2.7V$		15	mA
I_{CC}^3	Core quiescent current	$V_{CC} = 2.7V$, post 100 krads(Si)		5	mA
I_{CC}^3	Core quiescent current	$V_{CC} = 2.7V$, post 300 krads(Si)		400	mA
I_{CCIO}^3	I/O quiescent current	$V_{CCIO} = 3.6V$		50	μA
I_{CCIO}^3	I/O quiescent current	$V_{CCIO} = 3.6V$, post 100 krads(Si)		0.5	mA
I_{CCIO}^3	I/O quiescent current	$V_{CCIO} = 3.6V$, post 300 krads(Si)		5	mA
I_{REF}	DC supply current on INREF		-10	10	μA
I_{PD}	Pad Pull-down (programmable)	$V_{CCIO} = 3.6V$	-	150	μA

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Capacitance is sample tested for initial qualification or design changes only. Clock pins are 12pF maximum.

2. Input only or I/O. Duration should not exceed 1 second. Measured at initial qualification, or after any design or process change that may affect this parameter.

3. All quiescent current measurements utilize a worst case Standard Evaluation Circuit (SEC) which represents full utilization of synchronous, combinatorial and SRAM logic.

Table 5: DC Input and Output Levels¹

	INREF		V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
	V _{MIN}	V _{MAX}	V _{MIN}	V _{MAX}	V _{MIN}	V _{MAX}	V _{MAX}	V _{MIN}	mA	mA
LVTTTL	n/a	n/a	-0.3	0.8	2.0	V _{CCIO} + 0.3	0.4	2.4	2.0	-2.0
LVC MOS2	n/a	n/a	-0.3	0.7	1.7	V _{CCIO} + 0.3	0.7	1.7	2.0	-2.0
LVC MOS3	n/a	n/a	-0.3	0.8	2.0	V _{CCIO} + 0.3	.55	2.0	24.0	-24.0
LVC MOS3 ²	n/a	n/a	-0.3	0.8	2.0	V _{CCIO} + 0.3	0.20	V _{CCIO} - 0.2	0.10	-0.10
PCI	n/a	n/a	-0.3	0.3 x V _{CCIO}	0.5 x V _{CCIO}	V _{CCIO} + 0.5	0.1 x V _{CCIO}	0.9 x V _{CCIO}	1.5	-0.5

Notes:

1. The data provided in Table 5 are JEDEC and PCI specifications. See preceding AC Delay Data for information specific to Eclipse FPGA I/Os.
2. Low current mode for LVC MOS3 outputs.

Table 6: Max Bidirectional I/O per Device/Package Combination

Device	208 CQFP	288 CQFP	484 CLGA/484 CCGA
UT6325 Eclipse FPGA	99	163	316

Notes:

1. Excludes input only signals such as DEDCLK, PROGCLK and IOCTRL.

AC CHARACTERISTICS LOGIC CELLS (Pre/Post-Radiation)*(V_{CC} = 2.5V, T_A = 25°C, K=1.00)

SYMBOL	PARAMETER	Value (ns)	
		Min	Max
T _{PD}	Combinatorial Delay of the longest path: time taken by the combinatorial circuit to output	0.205	1.01
T _{SU}	Setup Time: time the synchronous input of the flip flop must be stable before the active clock edge	0.231	--
T _{HL}	Hold Time: time the synchronous input of the flip flop must be stable after the active clock edge	0	--
T _{CO}	Clock to Out Delay: the amount of time taken by the flip flop to output after the active clock edge	-	0.43
T _{CWHI}	Clock High Time: required minimum time the clock stays high	0.46	--
T _{CWLO}	Clock Low Time: required minimum that the clock stays low	0.46	--
T _{SET}	Set Delay: time between when the flip flop is "set" (high) and when the output is consequently "set" (high)	--	0.59
T _{RESET}	Reset Delay: time between when the flip flop is "reset" (low) and when the output is consequently "reset" (low)	--	0.66
T _{SW}	Set Width: time that the SET signal remains high/low	0.3	--
T _{RW}	Reset Width: time that the RESET signal remains high/low	0.3	

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Stated timing for typical case propagation delay over process variation at V_{CC}=2.5V and T_A=25°C. Multiply by the appropriate delay factor, K, for voltage and temperature settings as specified in operating range.
2. These limits are derived from a representative selection of the slowest paths through the logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

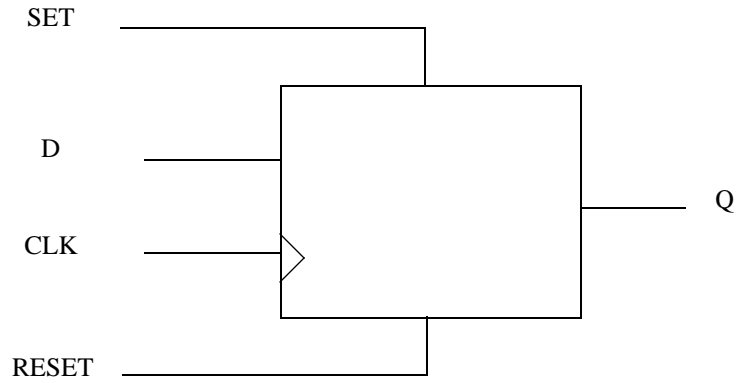


Figure 6: Logic Cell Flip Flop

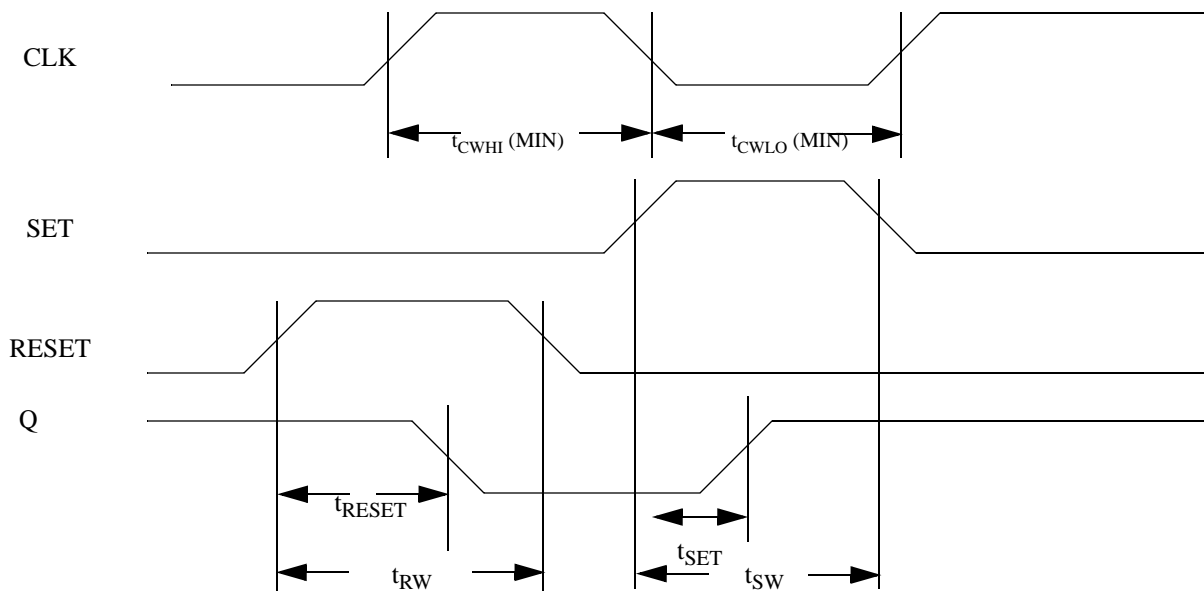


Figure 7: Logic Cell Flip Flop Timings - First Waveform

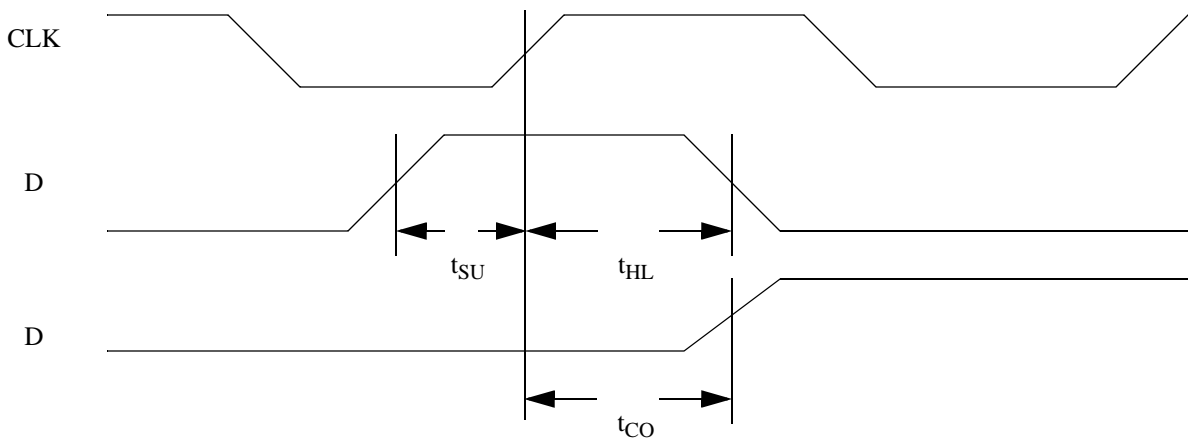


Figure 8: Logic Cell Flip Flop Timings - Second Waveform

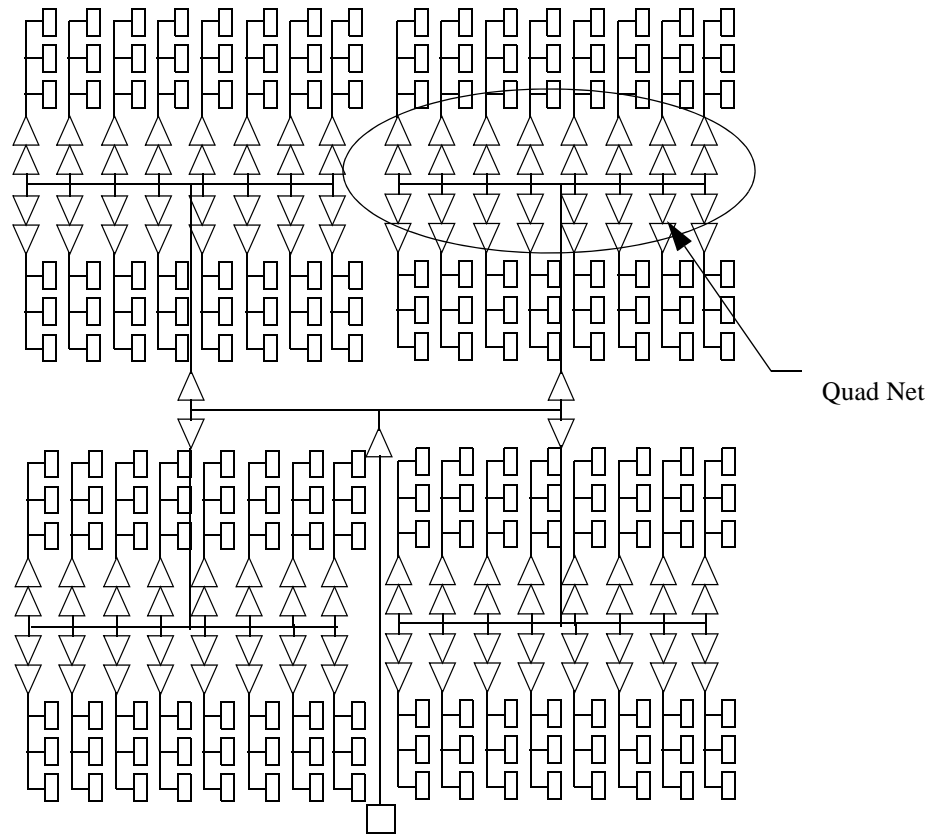


Figure 9: Global Clock Structure

GLOBAL CLOCK TREE DELAY

($V_{CC} = 2.5V$, $T_A = 25^{\circ}C$, $K=1.00$)

SYMBOL	PARAMETER	Value (ns)	
		Min	Max
t_{PGCK}	Global clock pin delay to quad net	0.990	1.386
t_{BGCK}	Global clock buffer delay (quad net to flip flop)	0.534	1.865

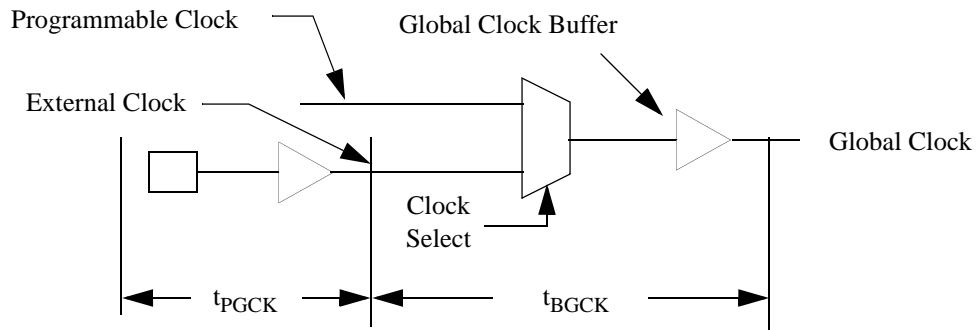


Figure 10: Global Clock Structure Schematic

RAM CELL SYNCHRONOUS and ASYNCHRONOUS READ TIMING

($V_{CC} = 2.5V$, $T_A = 25^{\circ}C$, $K=1.00$)

SYMBOL	PARAMETER	Value (ns)	
		Min	Max
RAM Cell Synchronous Read Timing			
t_{SRA}	RA setup time to RCLK: time the READ ADDRESS must be stable before the active edge of the READ CLOCK	0.686	--
t_{HRA}	RA hold time to RCLK: time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0	--
t_{SRE}	RE setup time to RCLK: time the READ ENABLE must be stable before the active edge of the READ CLOCK	0.243	--
t_{HRE}	RE hold time to RCLK: time the READ ENABLE must be stable after the active edge of the READ CLOCK	0	--
t_{RCRD}	RCLK to RD: time between the active READ CLOCK edge and the time when the data is delivered to RD	--	2.3
RAM Cell Asynchronous Read Timing			
t_{PDRD}	RA to RD: time between when the READ ADDRESS is input and when the DATA is output	--	2.4

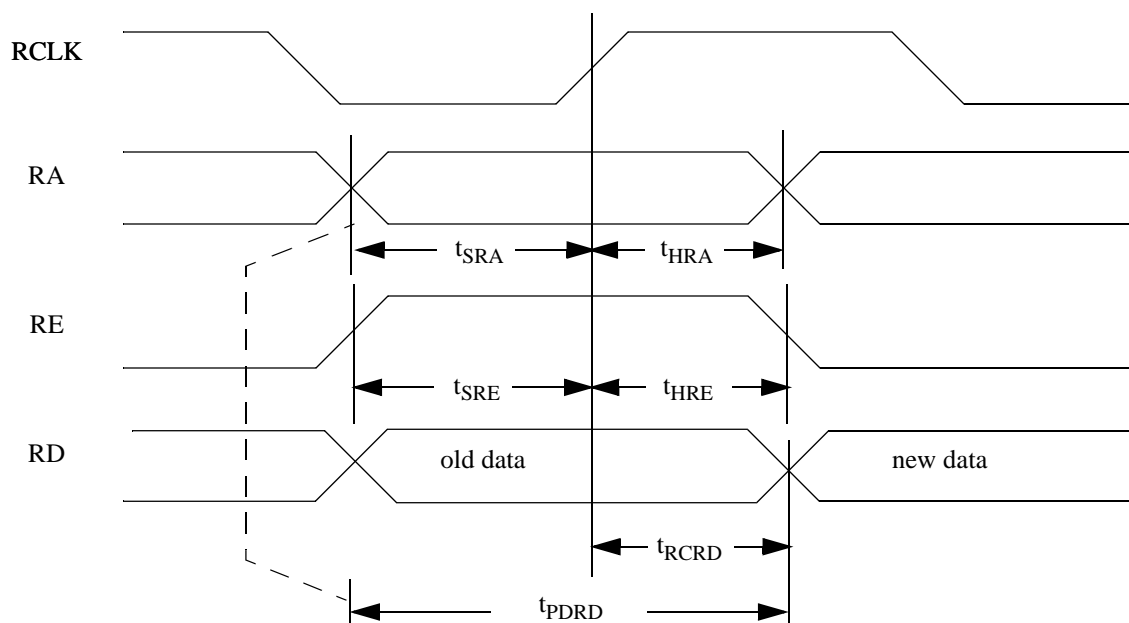


Figure 11: RAM Cell Synchronous and Asynchronous Read Timing

RAM CELL SYNCHRONOUS WRITE TIMING

($V_{CC} = 2.5V$, $T_A = 25^{\circ}C$, $K=1.00$)

SYMBOL	PARAMETER	Value (ns)	
		Min	Max
t_{SWA}	WA setup time to WCLK: time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	0.675	--
t_{HWA}	WA hold time to WCLK: time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0	--
t_{SWD}	WD setup time to WCLK: time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	0.654	--
t_{HWD}	WD hold time to WCLK: time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0	--
t_{SWE}	WE setup time to WCLK: time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	0.276	
t_{HWE}	WE hold time to WCLK: time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0	
t_{WCRD}	WCLK to RD (WA = RA): time between the active WRITE CLOCK edge and the time when the data is available at RD	--	2.8

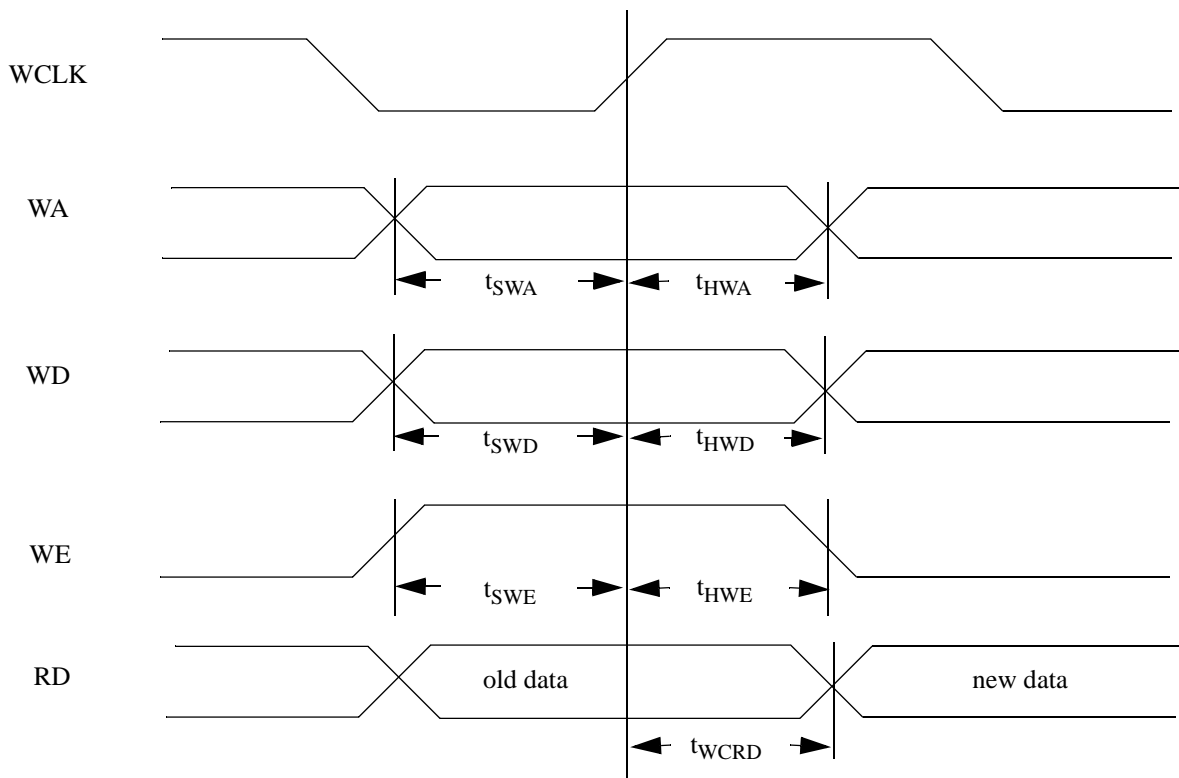


Figure 12: RAM Cell Synchronous Write Timing

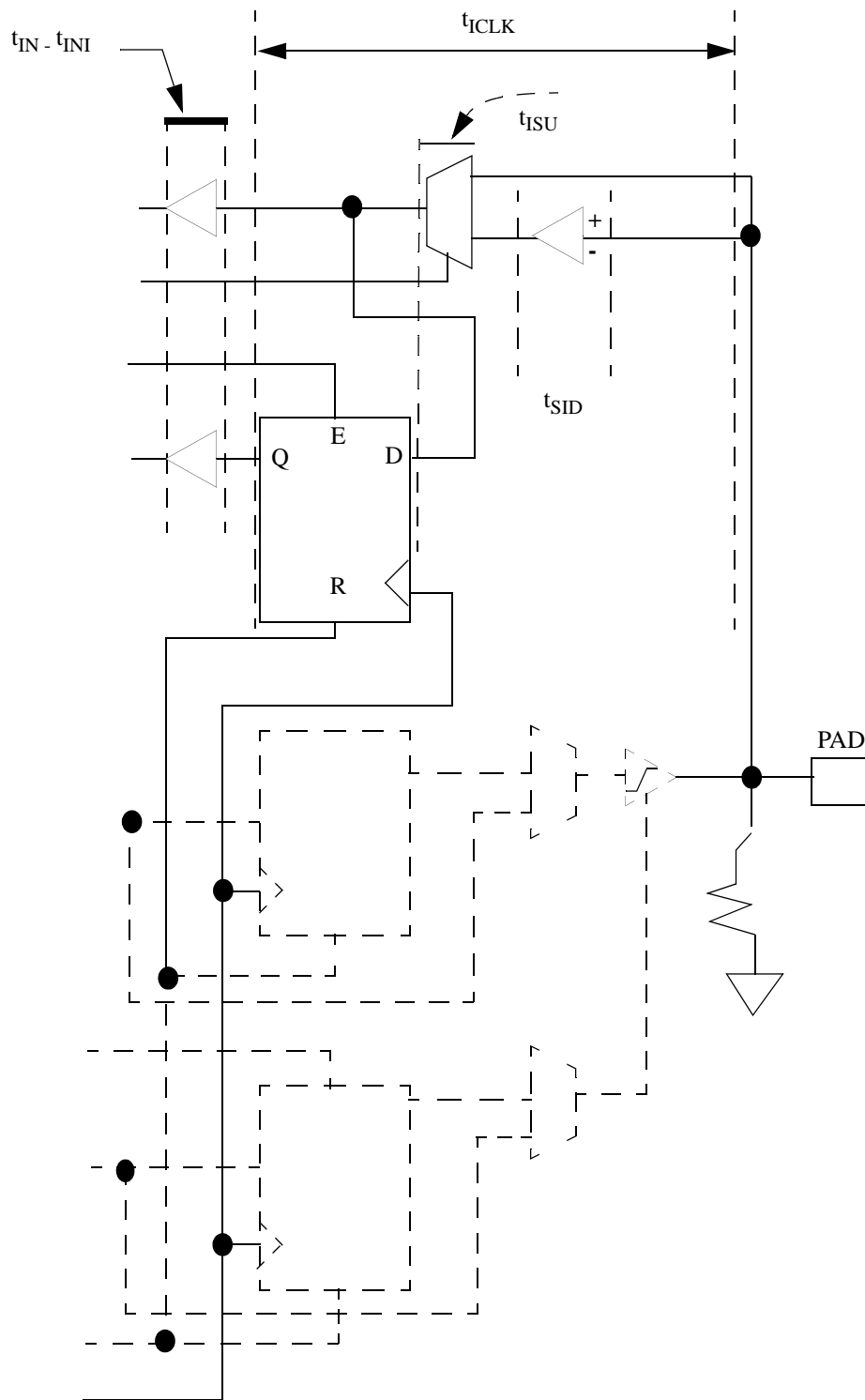


Figure 13. Input Register Cell

INPUT REGISTER CELL

($V_{CC} = 2.5V$, $T_A = 25^{\circ}C$, $K=1.00$)

SYMBOL	PARAMETER	Value (ns)	
		Min	Max
t_{ISU}	Input register setup time: time the synchronous input of the pin must be stable before the active clock edge	3.308	3.526
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0	--
t_{ICO}	Input register clock to out: time taken by the flip-flop to output after the active clock edge	--	0.494
t_{IRST}	Input register reset delay: time between when the flip-flop is "reset" (low) and when the output is consequently "reset" (low)	--	0.464
t_{IESU}	Input register clock enable setup time: time "enable" must be stable before the active clock edge	0.830	-
t_{IEH}	Input register clock enable hold time: time "enable" must be stable after the active clock edge	0	--

STANDARD INPUT DELAYS

($V_{CC} = 2.5V$, $T_A = 25^{\circ}C$, $K=1.00$)

SYMBOL	PARAMETER	Value (ns)	
		Min	Max
$t_{SID} (LVTTTL)$	LVTTTL input delay: Low voltage TTL for 3.3V applications	-	0.34
$t_{SID} (LVCMOS3)$	LVCMOS3 input delay: Low voltage CMOS for 3.3V applications	-	0.42

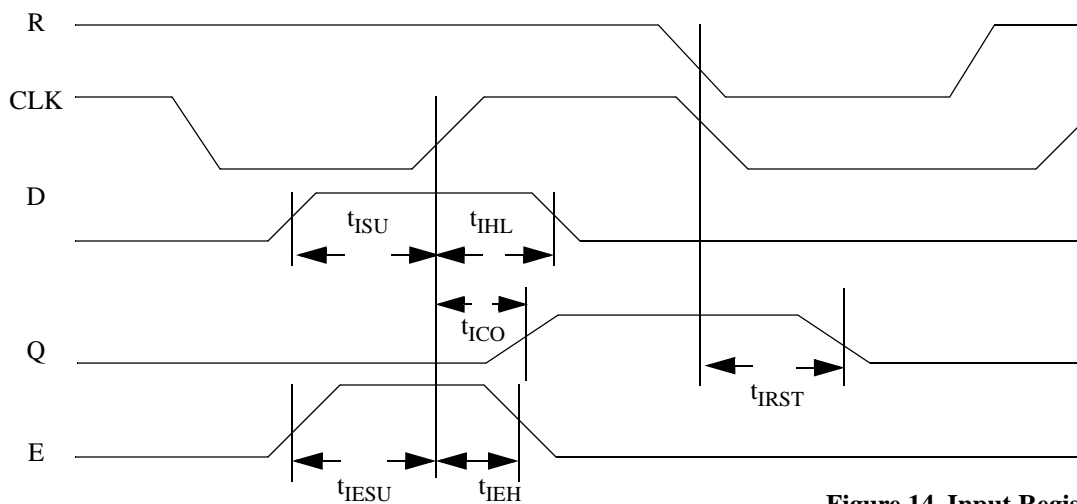


Figure 14. Input Register Timing

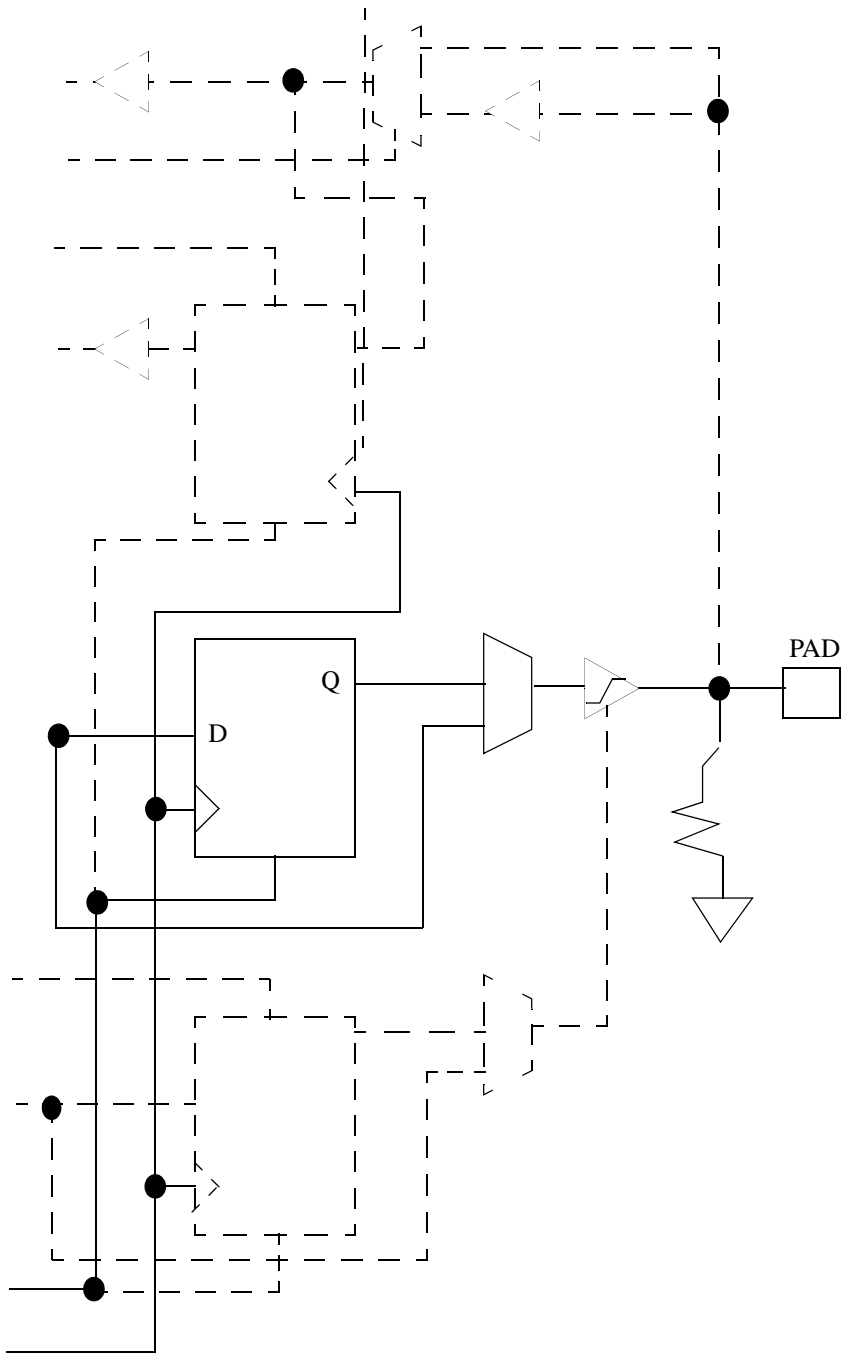


Figure 15. Output Register Cell

OUTPUT REGISTER CELL

($V_{CC} = 2.5V$, $T_A = 25^\circ C$, $K=1.00$)

SYMBOL	PARAMETER	Value (ns)	
		Min	Max
t_{OUTLH}	Output Delay low to high (90% of H)	-	2.59
t_{OUTHL}	Output Delay high to low (10% of L)	-	2.16
t_{PZH}	Output Delay tri-state to high (90% of H)	-	3.06
t_{PZL}	Output Delay tri-state to low (10% of L)	--	2.71
t_{PHZ}	Output Delay high to tri-state	--	3.44
t_{PLZ}	Output Delay low to tri-state	--	3.32
t_{COP}	Clock to out delay (does not include clock tree delays)	--	2.67 (fast skew) 9.0 (slow skew)

OUTPUT SLEW RATES

($V_{CC} = 2.5V$, $T_A = 25^\circ C$, $K=1.00$, $V_{CCIO} = 3.3V$)

	Fast Slew	Slow Slew
Rising Edge	2.8V/ns	1.0V/ns
Falling Edge	2.86V/ns	1.0V/ns

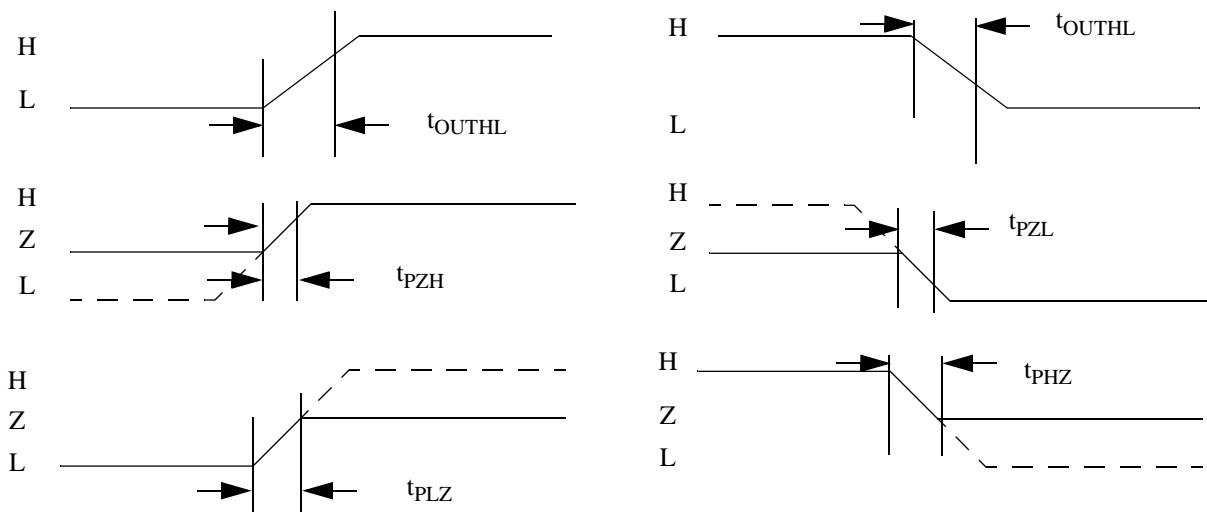


Figure 16. Output Register Cell Timing

Power vs Operating Frequency

The basic power equation which best models power consumption is shown below.

$$P_{\text{TOTAL}} = 0.350 + f(0.0031 N_{\text{LC}} + 0.0948 N_{\text{CKBF}} + 0.01 N_{\text{CLBF}} + 0.0263 N_{\text{CKLD}} + 0.543 N_{\text{RAM}} + 0.0035 N_{\text{INP}} + 0.0257 N_{\text{OUTP}}) \text{ (mW)}$$

Where

- N_{LC} is the total number of logic cells in the design
- N_{CKBF} = # of clock buffers
- N_{CLBF} = # of column clock buffers
- N_{CKLD} = # of loads connected to the column clock buffers
- N_{RAM} = # of RAM blocks
- N_{INP} is the number of input pins
- N_{OUTP} is the number of output pins

Figure 17 exhibits the power consumption in the device. The chip was filled with (300) 8-bit counters, approximately 76% logic cell utilization.

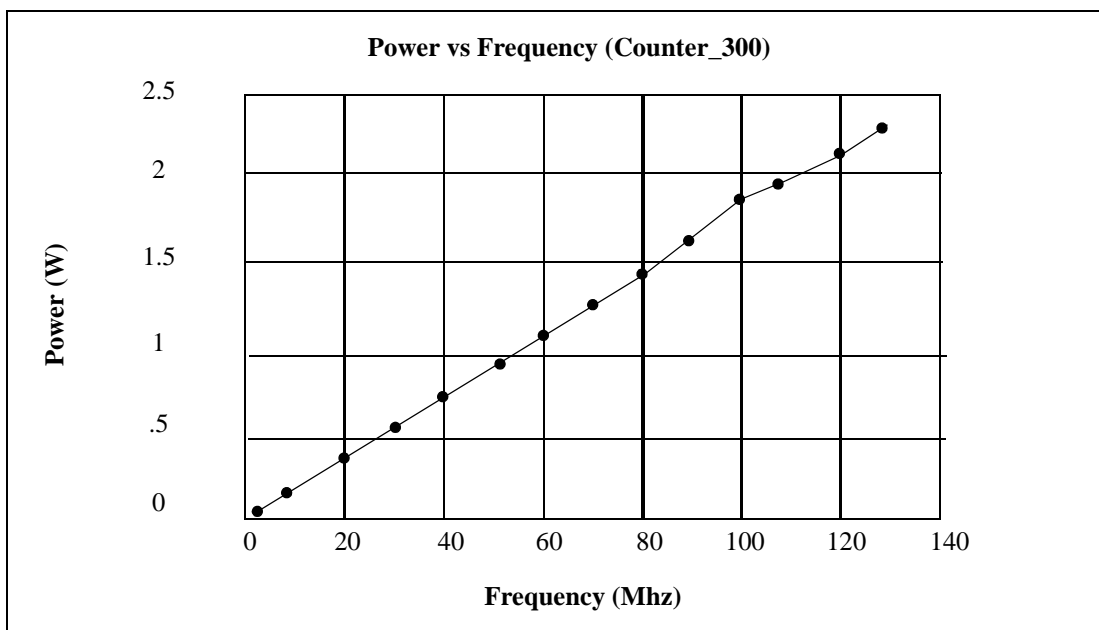


Figure 17: Power Consumption

Power-Up Sequencing

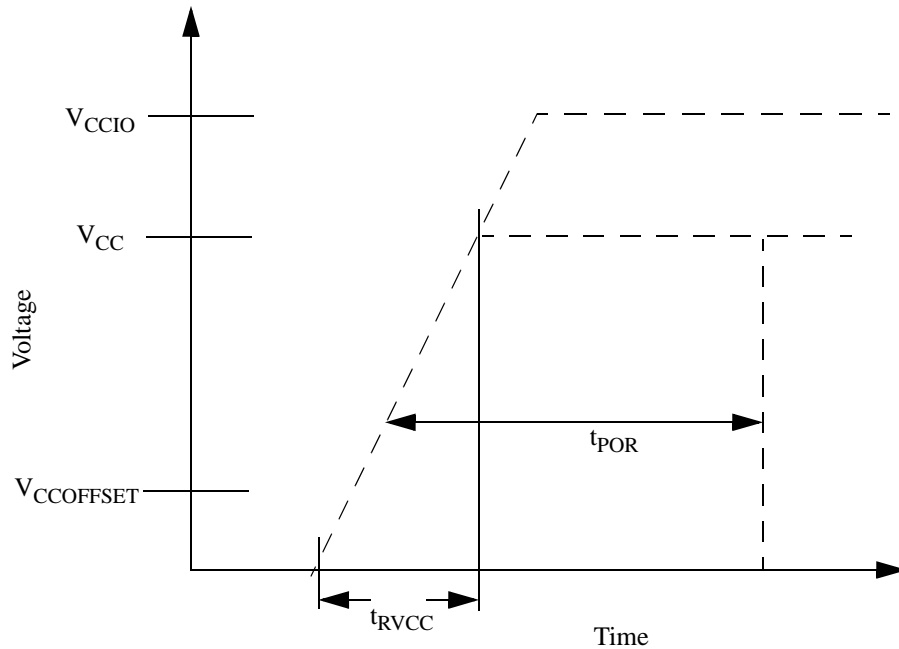


Figure 18. Power-Up Requirements/Recommendations

Notes:

1. V_{CC} and V_{CCIO} should either be ramped simultaneously to their final values (as shown) or with the core voltage V_{CC} leading the I/O voltage V_{CCIO} .
2. Rise time for the voltage supplies (t_{RVCC}) must be within the range of $1\mu s < t_{RVCC} < 200ms$.
3. Voltage power up/power down ramps for the supplies must be monotonically increasing/decreasing.
4. The starting point for power up ($V_{CCOFFSET}$) must be less than or equal to 300mV.
5. Users must allow time for the asynchronous power on reset to complete initialization of the device (t_{POR}). For fast rise times, ($t_{RVCC} < 10msec$) a minimum $t_{POR} = 10 msec$ must be allowed. For slower rise times, $10ms < t_{RVCC} < 200ms$, a minimum $t_{POR} = t_{RVCC}$ must be allowed.

Joint Test Access Group (JTAG)

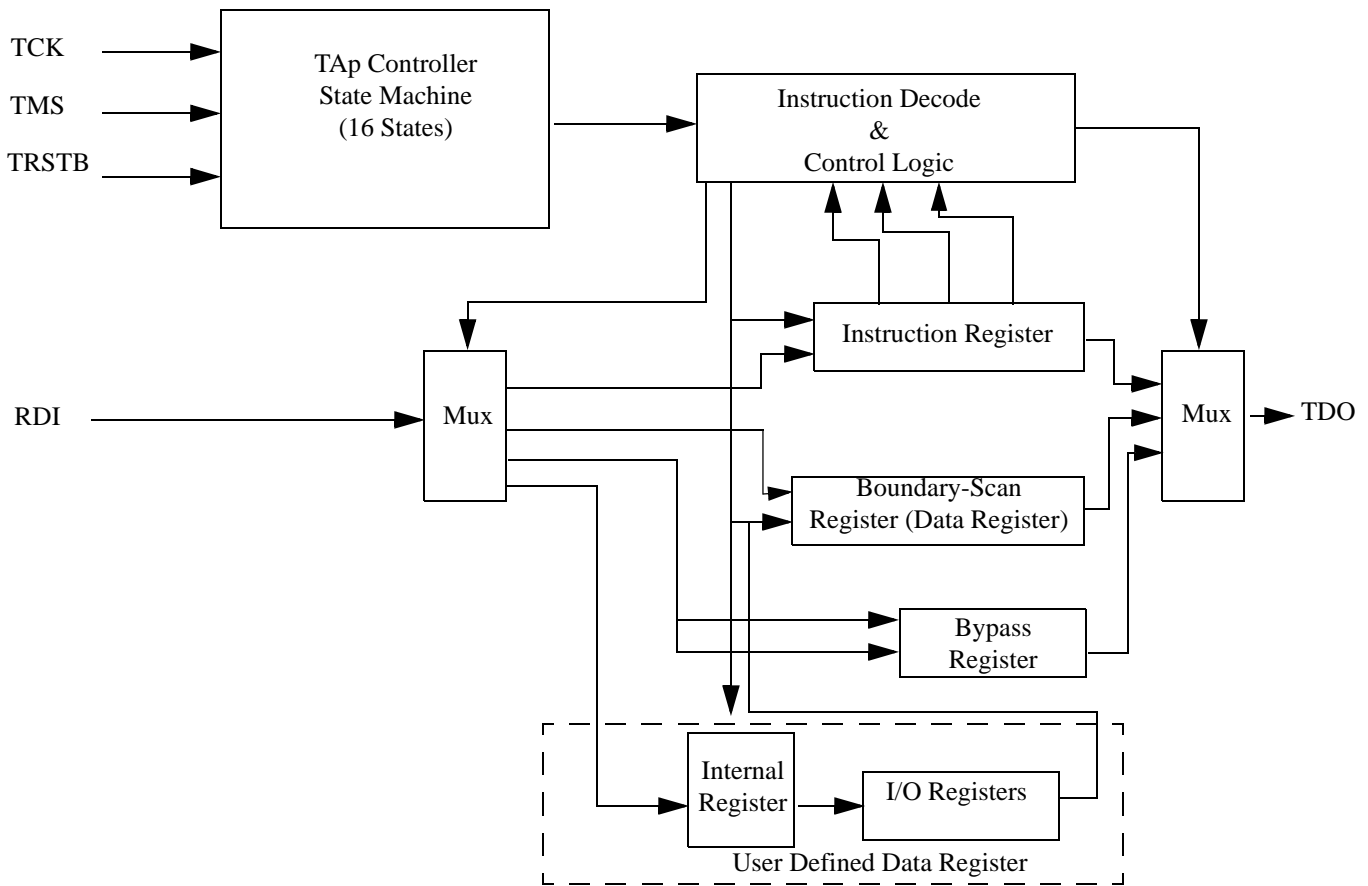


Figure 19. JTAG Block Diagram

Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, not in the least of which concerns the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR), which allow users to run three required tests along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction:** The Extest instruction performs a PCB interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP's Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction:** This instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed

via a data scan operation, allowing users to sample the functional data entering and leaving the device.

- **Bypass Instruction:** The Bypass instruction allows data to skip a device’s boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

Table 7: JTAG Pin Descriptions

Pin	Function	Description
TDI/RSI	Test Data In for JTAG/RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to V _{CC} if unused.
TRSTB/RRO	Active low Reset for JTAG/RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM data in for RAM initialization. Connect to GND if unused.
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to V _{CC} if not used for JTAG.
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to V _{CC} or GND if not used for JTAG.
TDO/RCO	Test data out for JTAG/RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization.

Recommended Unused Pin Terminations for the UT6325 Eclipse FPGA Devices

All unused, general purpose I/O pins can be tied to V_{CC}, GND, or HIZ (high impedance) internally using the Configuration editor. This option is given in the bottom-right corner of the placement window. To use the Placement Editor, choose **Constraint ->Fix Placement** in the Option pull-down menu of SpDE. The rest of the pins should be terminated at the board level in the manner presented in Table 8.

Table 8: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
IOCTRL <y>	Any unused pins of this type should be connected to either V_{CC} or GND (recommended: GND).
CLK/PLLIN <x>	Any unused clock pins should be connected to either V_{CC} or GND (recommended: GND).
INREF <y>	If an I/O bank does not require the use of an INREF signal, that INREF pin should be connected to GND.
V_{CCPLL} <x>	If a PLL is not used, the associated V_{CCPLL} must be connected to the same voltage as PLLRST (2.5V or GND; recommend GND).
PLLRST <x>	If a PLL is not used, the associated PLLRST must be connected to the same voltage as V_{CCPLL} (2.5V or GND; recommend GND).
PLLOUT <x>	Unused PLLOUT pins must be connected to either V_{CC} or GND so that the input buffer portion never floats (recommend GND). Utilized PLLs which route the PLL clock outside of the chip require use of the associated PLLOUT pin.

Note: X---> number, Y ---> alphabetical character

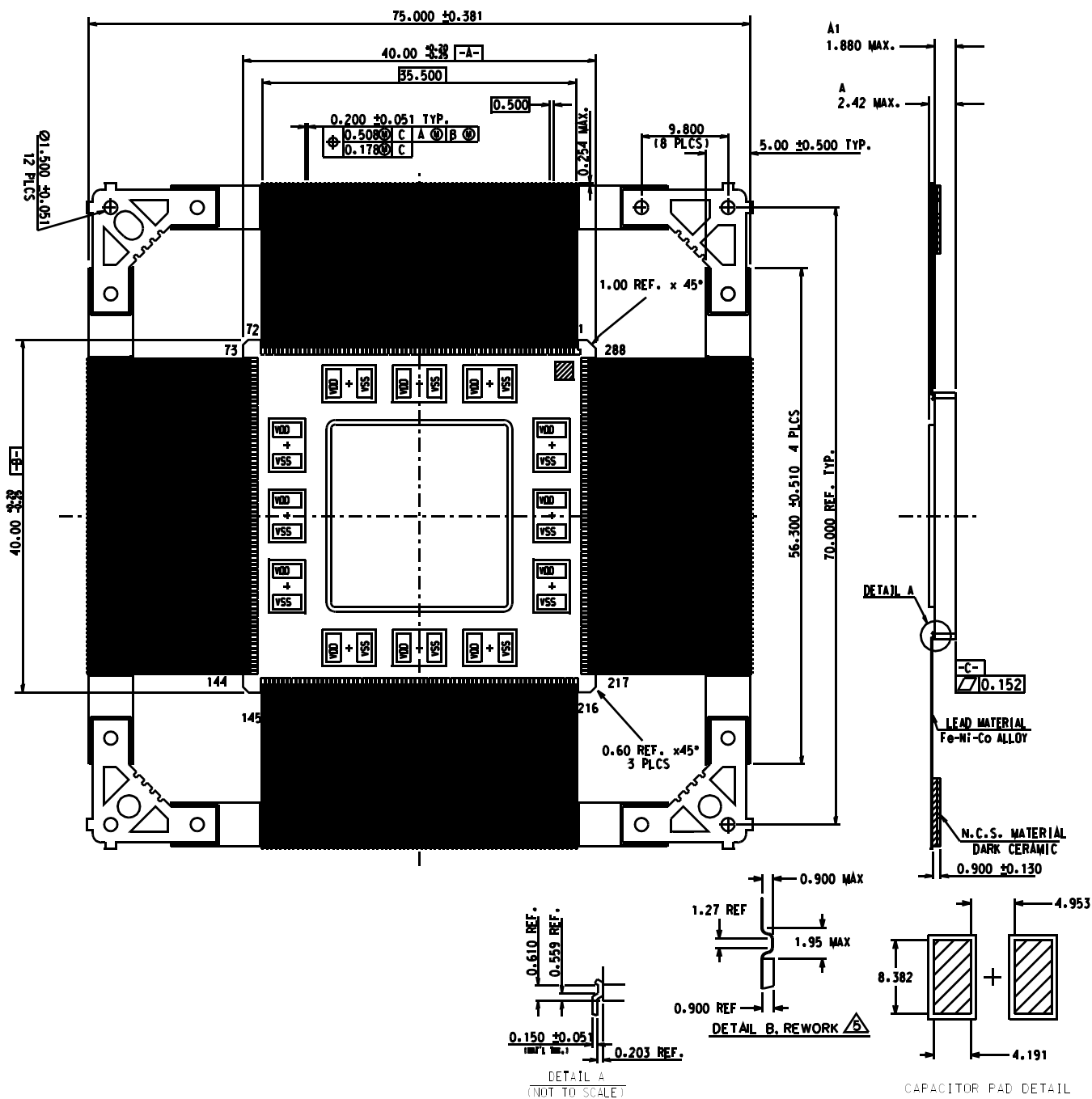
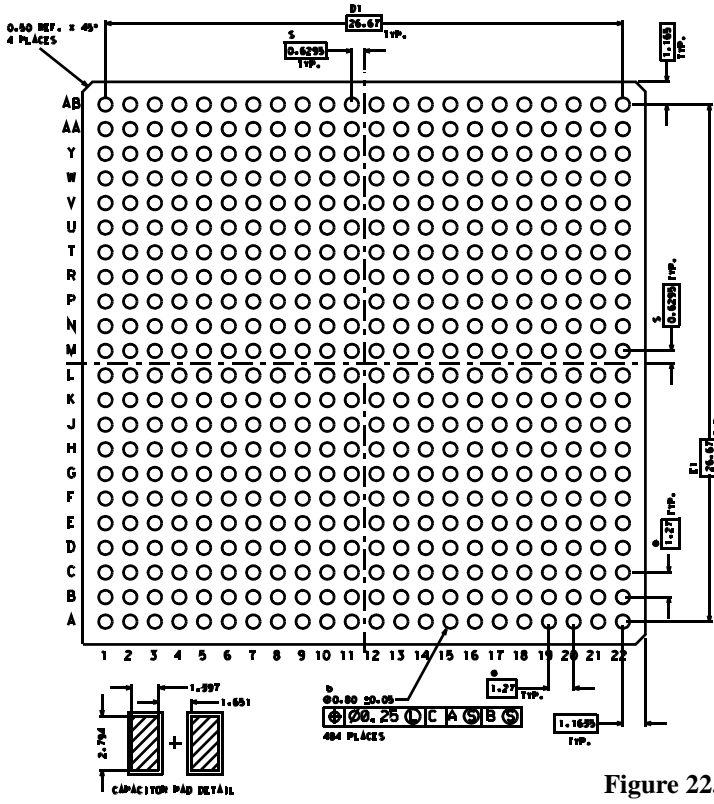
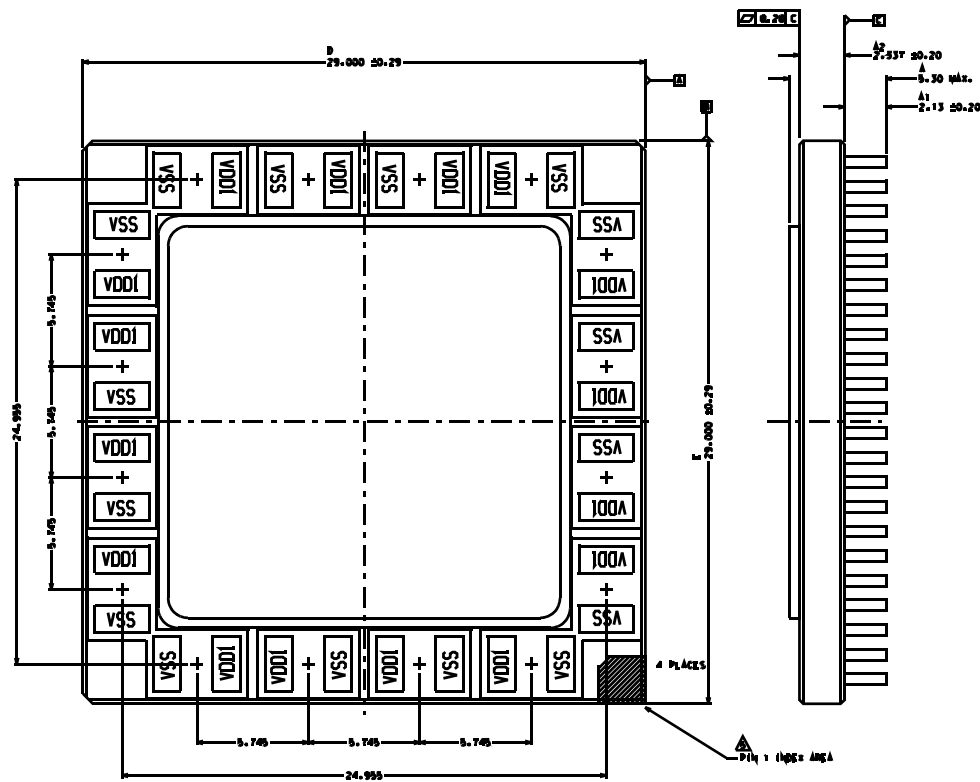


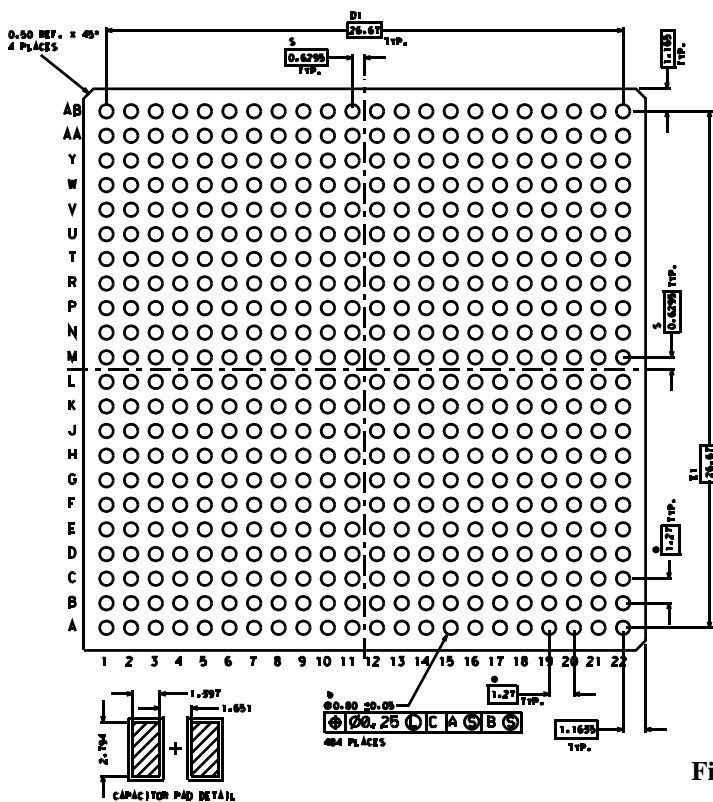
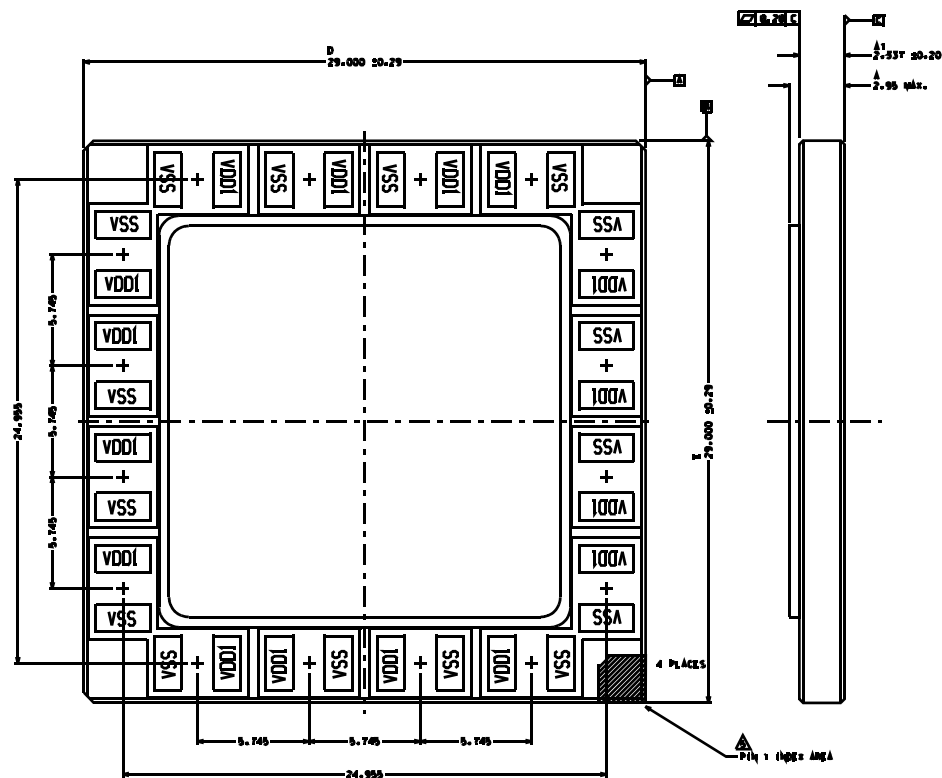
Figure 21. 288-pin Ceramic Quad FLATPACK

1. All exposed metalized areas are gold plated over nickel plating per MIL-PRF-38535.
2. App note: Capacitor monitoring pads are dimensioned for a MIL-C-55581 CDR33 chip capacitor.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Letter designations are to cross-reference to MIL-STD-1835.
5. Packages may be shipped with repaired leads as shown. Coplanarity requirements do not apply in repaired area.
6. Seal ring is connected to V_{SS} .
7. Drawing units are in millimeters.



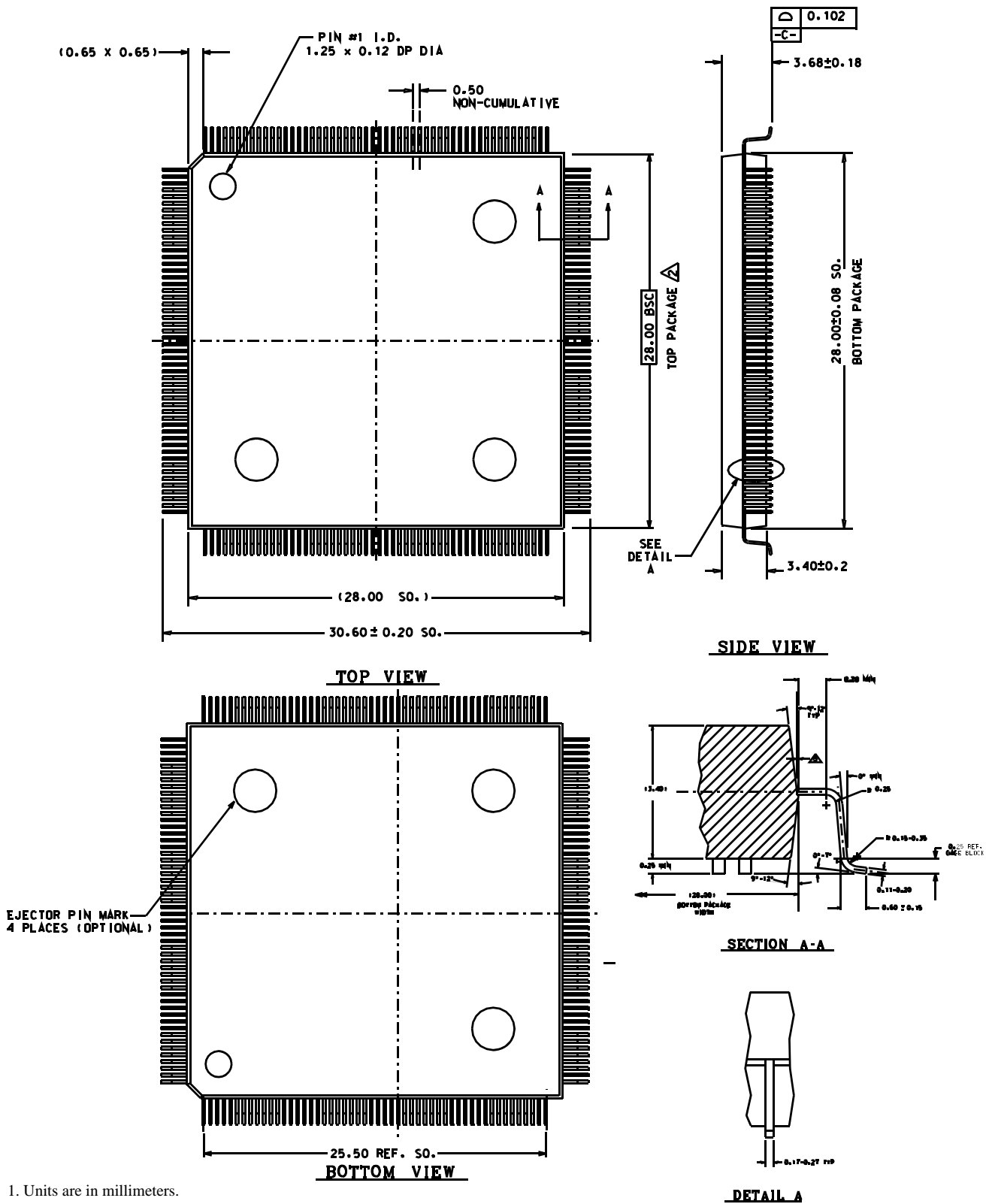
1. Seal ring is connected to V_{SS} .
2. Units are in millimeters (inches).
3. All top sides exposed metalized areas must be gold plated 100 to 225 micro-inches thick and all bottom side exposed metalized areas must be gold plated to 60 micro-inches thick nominal. Both sides shall be over electroplated nickel undercoating 100 to 350 micro-inches per MIL-PRF-38535. The bottom side plating is not subject to the salt atmosphere requirements of 40-7150-xx.
4. Camber: 0.08MM max.
5. Geometry is vendor optional. Cannot be alphanumeric and must be isolated within the shaded area. Must be electrically isolated. Plating is optional.

Figure 22. 484-pin Ceramic Column Grid Array



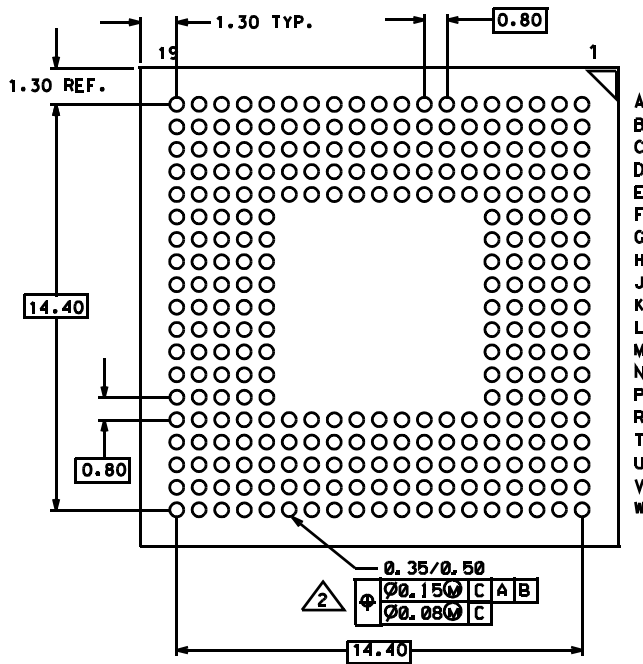
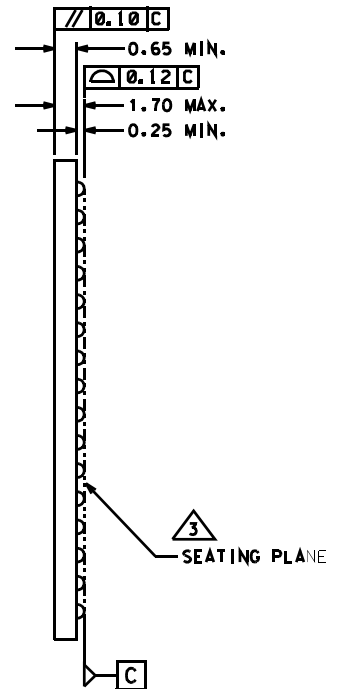
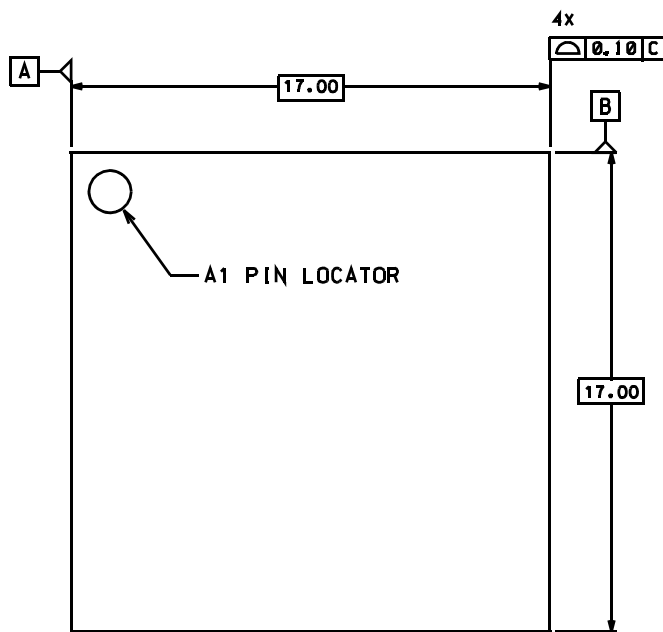
1. Seal ring is connected to V_{SS} .
2. Units are in millimeters (inches).
3. All top sides exposed metalized areas must be gold plated 100 to 225 micro-inches thick and all bottom side exposed metalized areas must be gold plated to 60 micro-inches thick nominal. Both sides shall be over electroplated nickel undercoating 100 to 350 micro-inches per MIL-PRF-38535. The bottom side plating is not subject to the salt atmosphere requirements of 40-7150-xx.
4. Camber: 0.08MM max.
5. Geometry is vendor optional. Cannot be alphanumeric and must be isolated within the shaded area. Must be electrically isolated. Plating is optional.

Figure 23. 484-pin Ceramic Land Grid Array



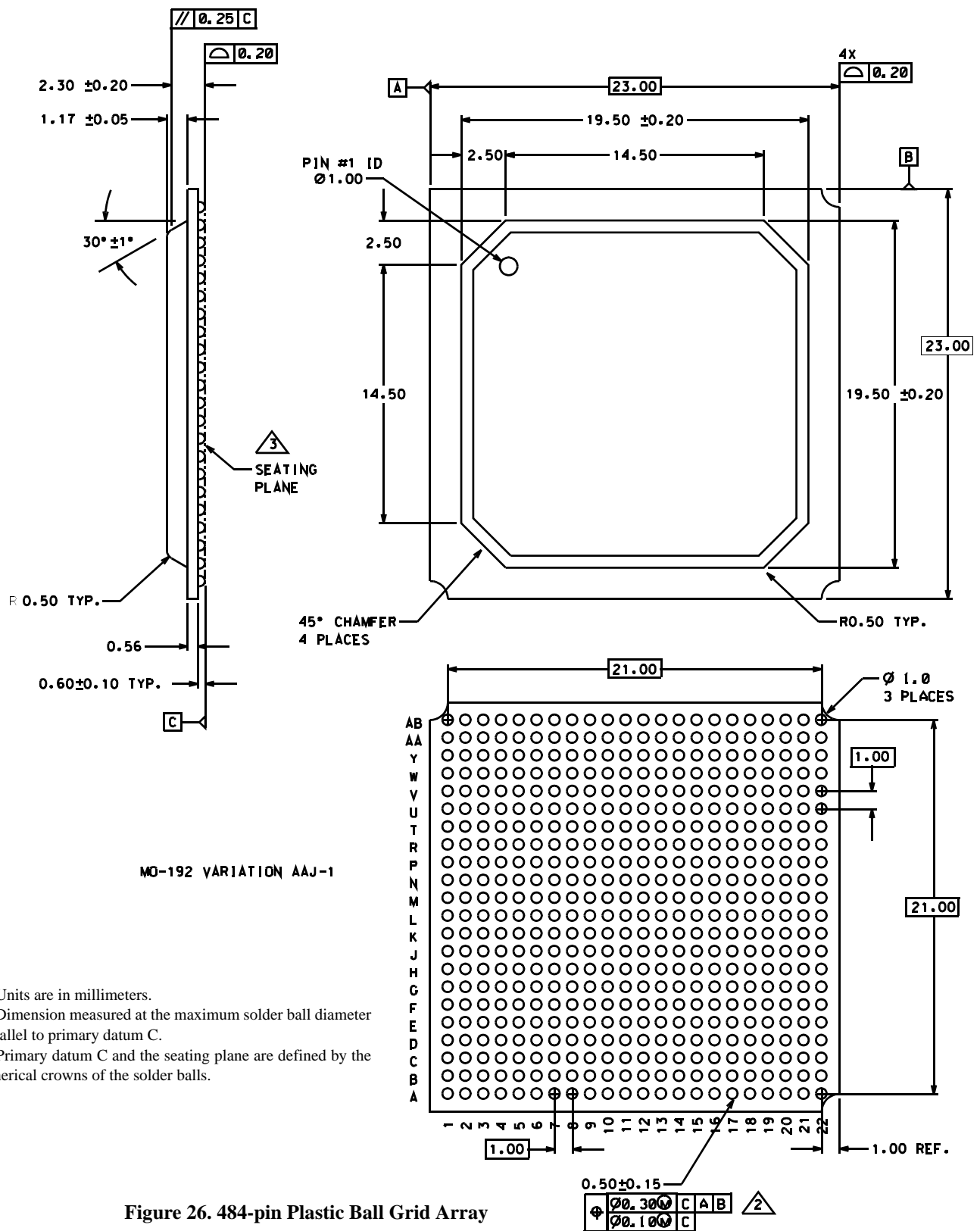
1. Units are in millimeters.
2. The top package body size may be smaller than the bottom package body size by as much as 0.20.
3. Body mold protrusion of 0.25 max per side is allowed.
4. Lead finish is tin-lead plated.

Figure 24. 208-pin Plastic Quad Flat Pack



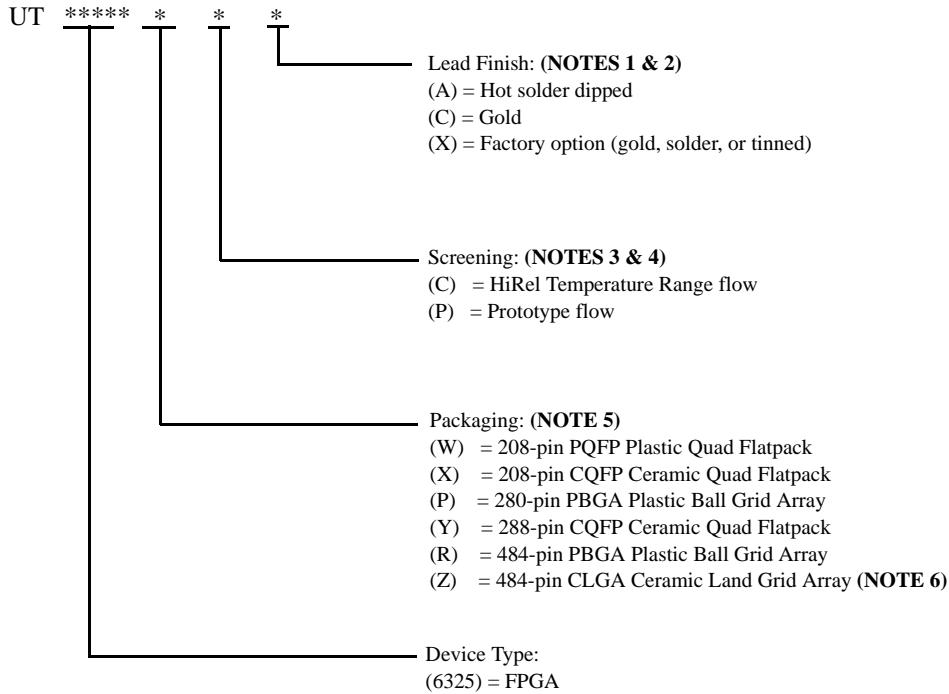
1. Units are in millimeters.
2. Dimension measured at maximum solder ball diameter parallel to primary Datum C.
3. Primary Datum C and the seating plane are defined by the spherical crowns of the solder balls.

Figure 25. 280-pin Plastic Ball Grid Array



ORDERING INFORMATION

UT6325 RadTol Eclipse FPGA:

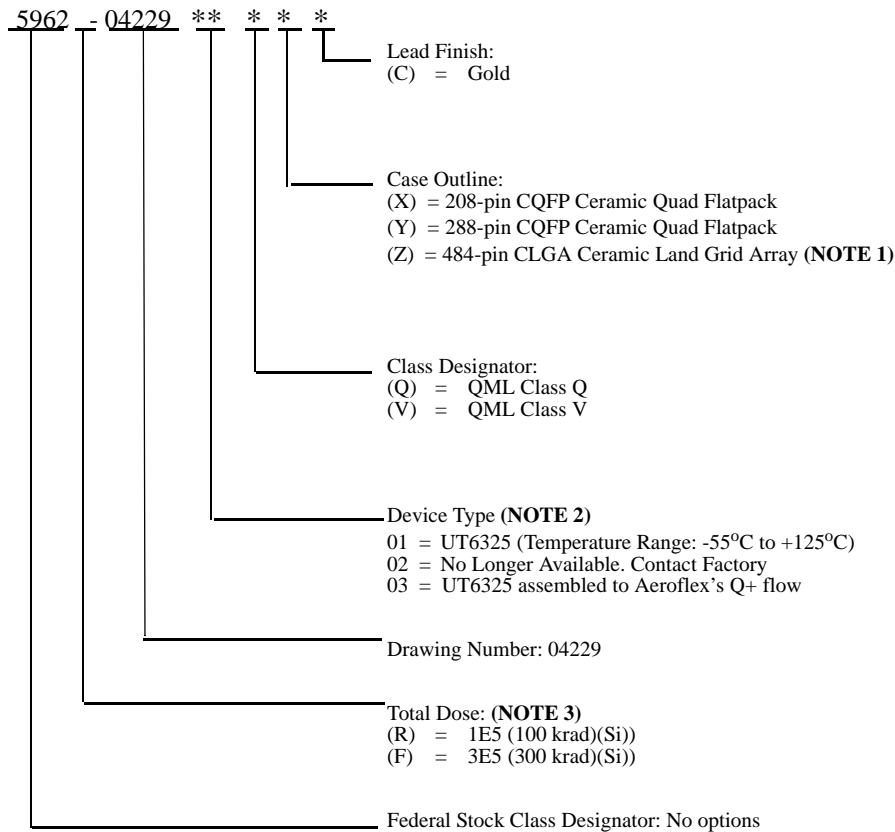


Notes:

- Lead finish (A, C, or X) must be specified.
- If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- Prototype flow per Aeroflex Manufacturing Flows Document. Tested at 25°C only. Lead finish is FACTORY OPTION "X" only. Radiation neither tested nor guaranteed.
- HiRel Temperature Range flow per Aeroflex Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.
- Use the following table to determine which lead finishes to select for the corresponding package options.
- Aeroflex offers COLUMN ATTACHMENT as an additional service for the ceramic land grid array (Case Outline "Z"). If needed, please ask for COLUMN ATTACHMENT when submitting your request for quotation.**

Package Option	Associated Lead Finish Option
(W) 208-PQFP	(A) Hot Solder Dipped
(X) 208-CQFP	(C) Gold
(P) 280-PBGA	(A) Hot Solder Dipped
(Y) 288-CQFP	(C) Gold
(R) 484-PBGA	(A) Hot Solder Dipped
(Z) 484-CLGA	(C) Gold

UT6325 FPGA: SMD



Notes:

1. Aeroflex offers COLUMN ATTACHMENT as an additional service for the ceramic land grid array (Case Outline "Z"). If needed, please ask for COLUMN ATTACHMENT when submitting your request for quotation.
2. Aeroflex's Q+ assembly flow, as defined in section 4.2.2.d of the SMD, provides QML-Q product through that SMD that is manufactured with Aeroflex's standard QML-V flow.
3. Aeroflex's Total dose radiation must be specified when ordering. QML Q not available without radiation hardening.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced HiRel

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Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused