

QCOTS™ UT8SDMQ256M8 2 Gigabit SDRAM

Data Sheet
April 16, 2004



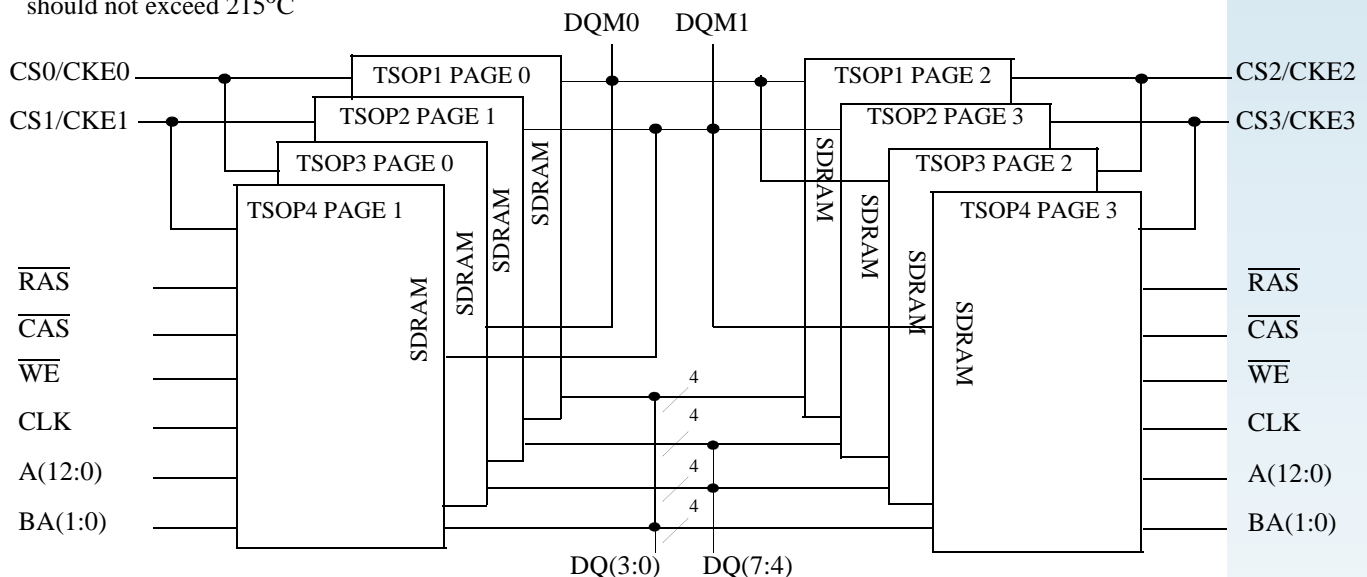
FEATURES

- ❑ Organized 256M x 8bits
- ❑ Single JEDEC standard 3.3V power supply
- ❑ 33MHz operation -40°C to 85°C
- ❑ LVTTTL compatible with multiplexed address
- ❑ Four bank operation
- ❑ MRS cycle with address key program
 - CAS latency (2 and 3)
 - Burst length (8)
 - Burst type (sequential and interleave)
- ❑ Fully synchronous; all signals registered on positive edge of system clock
- ❑ Burst read single-bit write operation
- ❑ Clock suspend mode
- ❑ Auto-refresh and self-refresh
- ❑ Typical radiation performance
 - Total dose > 10krad(Si)
 - SEL Immune >40-60 MeV-cm²/mg (contact factory)
- ❑ Package options:
 - 68-lead ceramic bottom brazed quad flatpack
- ❑ Max temperature at module side during installation should not exceed 215°C

INTRODUCTION

The UT8SDMQ256M8 is a high performance, highly integrated Synchronous Dynamic Random Access Memory (SDRAM) non-hermetic MSM (Multi-Stack Module) incorporating stack technology. Total module density is 2,147,483,648 bits of storage. Each module consists of two 1GB stacks. Each 1GB stack contains two (2) 512M bit pages, organized 64M by 8 bits (pages are organized as four (4) banks of 16M x 8 selected via BA(1:0)). The four pages have an 8-bit interface independently selectable using the appropriate active-low chip select pin (\overline{CS}_n). All other signals are common to the eight (8) 256 Mbit SDRAM memories. Synchronous design allows precise memory accesses through the use of two system clocks. This architecture provides the ability for I/O transactions being performed on the positive edge of each clock cycle.

Ideal uses for the UT8SDMQ256M8 include space applications requiring high performance and high density, such as a space borne solid state recorder. In addition, the programmable burst length and programmable \overline{CAS} latencies enable the device to be used in a variety of high bandwidth space applications.



Common Signals: \overline{RAS} , \overline{CAS} , \overline{WE} , CLK, A(12:0) and BA(1:0)

Figure 1: UT8SDMQ256M8 Functional Block Diagram (2Gb MODULE)